9. CONCLUSIONS.

In this thesis the theory of wave filters has been extended and a novel implementation of filters based on this approach has been designed and developed. An integrated circuit containing three of these filters has been fabricated using a sampled-data analogue technique in which values are held as voltages on, or charges in, capacitors.

The theoretical aspects of wave filters have been examined in chapter three and the computer simulation program described in chapter four has shown that use of this theory does produce very exact filter responses.

The sampled-data analogue technique introduced in chapter five and used to implement the filters does introduce some discrepancies between the practical filter response and the exact filter response which are due to the effects of stray capacitances in the circuit. However, with careful design and particularly if some attempt is made to compensate for the effects of the stray capacitances, as described in section 5.2, an acceptable filter response can still be obtained.

The bulk of this work has been concentrated on wave filters which model cascaded transmission line networks using two-port adaptors, but in chapter six the feasibility of the sampled-data analogue technique for filters using three-port adaptors has been demonstrated in some original work. In the opinion of the author the practical application
of wave filters will inevitably require the use of multi-port adaptors and future work should be concentrated in this area.

In chapter seven an integrated circuit containing three wave filters based on a cascaded unit element reference network was described. The main aim of this work has been to achieve a specified amplitude response for the filters, and it can be seen from the results presented in chapter eight that this has indeed been achieved.

There are significant problems associated with this IC. The first is its physical size which, at 5 by 6 mm$^2$ is large by the standards of today. The second, and more serious, problem is the poor dynamic range of the filters.

The integrated circuit designed in this work is large for three reasons.

1. The circuit uses full operational amplifiers whereas only single-ended buffer amplifiers are required.

2. Only half the number of buffer amplifiers actually used are needed.

3. The capacitors used in the circuit are very large.

The first problem would be greatly eased by the use of a **CMOS** process which would, by incorporating fewer transistors in the circuit, permit the fabrication in a very small
layout area of genuine single-ended buffers which had a gain of very close to one.

The second problem can be removed by noting that each buffer is only required during one clock cycle; during the other clock cycle it is inoperative. Therefore no speed penalty would be incurred if one buffer was multiplexed between two positions in the circuit. This would reduce the number of buffers required by half.

Regarding the third problem of capacitor size which is directly related to the high values of the capacitors used, this is a trade-off between the advantage of an exact amplitude response and the advantages of circuit speed, low power consumption and low layout area. If the capacitor sizes are reduced then the stray capacitances will have a greater effect on the amplitude response of the filter which may then begin to deteriorate significantly. However, the speed of the circuit will increase when smaller capacitors are used and the power consumed by the circuit will decrease, as will the layout area occupied by the filter.

The main difficulty inherent in these filters is their poor dynamic range which can only be improved in two ways: by increasing the maximum signal level or decreasing the filter noise level.

The maximum signal input level for the filter can be increased by scaling the signal within the adaptors, as briefly described at the end of section 8.4.2, and by the
use of a CMOS process which will allow the buffers to output larger signals. Before this class of filter becomes very useful these steps must be taken to improve the dynamic range.

The filter noise level could be reduced by careful design of the buffers, which are the main noise source in these structures. It must also be remembered that reducing the size of the capacitors in the circuit will lead to higher values of $kT/C$ noise being produced which could result in this source of noise becoming significant.

To give some idea of the possible parameters of designs that could be implemented using the techniques described in this thesis let us consider a re-design, using a CMOS process, of the seventh order filter that has already been integrated in this work. The filter design would differ from the one already integrated in the following ways.

1. The buffer amplifiers would be multiplexed and would be genuine single-ended unity gain amplifiers rather than the full operational amplifiers used at present. If possible a facility for adjusting the gain of the buffers would be built into the circuit in order to permit adjustment of the peaking of the filter amplitude response. There would be half as many buffers as there are at present, they would each consume less power than the NMOS operational amplifiers now used and they would amplify
signals over the full power supply range.

2. The capacitors used in the circuit would all be from layers P1 to P2 to remove any voltage dependent effects. They would be ratioed using the technique briefly described in the part of section 7.3.2 which deals with P1 to P2 capacitors, and would be smaller in value and hence occupy less layout area than those in the circuit already designed.

3. If possible some primitive form of signal scaling would be built into the filter to increase the maximum possible input signal. This would only be possible if the tolerances on the scaling form were very tightly defined.

4. More attention would be given to the noise sources in the filter with a view to their reduction or elimination. Using these techniques the dynamic range of the filter would be greatly improved. Use of CMOS buffers alone would increase the dynamic range by 9.5dB even if all the other points had no effect.

There are two other techniques available for the production of integrated filters; Switched-Capacitor filters and digital filters, both discussed in chapter two. The main advantage the sampled-data analogue wave filter has over the Switched-Capacitor filter is that its amplitude response is
exact. However, some recent work [61] has shown some encouraging results in the production of exact low-pass responses using Switched-Capacitor techniques. It is likely that similar results will be found for the other classes of filter, for example band-pass, that are required.

With the advent of VLSI it is inevitable that digital techniques will become dominant in integrated filter design. As one micron and sub-micron processes become available it will be possible to include extremely complex algorithms on chip and, in the opinion of the author, nearly all filtering will be achieved using digital techniques. The reduction in process minimum geometries which will make this possible is of little help to the analogue filter designer, as lowered transistor sizes imply higher noise levels [62] which reduce the dynamic range of the circuit. Increased noise levels are, however, of little importance to digital circuits which can give acceptably low error rates with a signal to noise ratio as low as 20dB. A digital filter has the further advantage that it can achieve any desired dynamic range simply by increasing its word length. The high power consumed by digital circuits, one of their significant disadvantages at present, will be greatly reduced by the use of sub-micron CMOS technology.

It will be remembered from chapter three that wave filter theory is independent of the filter realisation chosen. This can be seen, for example, by the fact that in this thesis analogue techniques have been used though the filter was
originally thought of as a digital structure. Because of this, and the advantage of low coefficient sensitivity present in wave filters regardless of the implementation used, it is likely that in the future, when the circuit complexity required can be accommodated on one chip, wave filters will be a very prominent subset of digital filters.

In conclusion, it has been shown in this thesis that sampled-data analogue techniques can be used to realise wave filters and that these wave filters should be another useful weapon in the armoury of the filter designer. It is admitted that the useful life of this analogue realisation of the wave filter may be short as advances in processing technology permit the use of increasingly smaller device geometries and therefore more and more complex digital filter structures. In time only digital structures may be used, but even then the wave filter will have a part to play as it will still enjoy, in a digital circuit, the many advantages it has in an analogue implementation.