7. INTEGRATED CIRCUIT DESIGN.

7.1 SPECIFICATIONS.

An Integrated Circuit (IC) was to be designed to validate the wave filter concept based on the novel implementation advocated in this research. The IC was to include the following features.

1. It was to contain three completely independent wave filters of the two-port adaptor type described in chapter five. These filters were to be of third, fifth and seventh order.

2. Each filter was to have a Chebyshev response with a designed cutoff frequency of one eighth of the clocking frequency. The microwave reference filters on which the wave filters were based were to have pass-band VSWR's of 1.5:1. This implies a designed pass-band ripple of 0.177dB for the wave filters. (See equations 3.31.)

3. The maximum clocking frequency to be aimed at was to be 60kHz.

4. Four phase clocking was to be used. This feature separated each of what had been $\varnothing 1$ and $\varnothing 2$ into two further clock pulses so that the output from one adaptor is created in one clock phase and given to the next adaptor in the next phase. The structure is still essentially two phase in that the calculations are performed in two stages, the
only difference being that each calculation now takes two clock pulses. This modified clocking scheme is shown in Fig. 7.1.

Figure 7-1: Four phase clocking scheme applied to a cascade of two two-port adaptors.

The four clock wires were to be made available as external connections, which allowed the filter to be driven in the two phase mode by simply connecting the correct pairs of clock wires together. This was, in fact, done and all the results that will be given in this text apply to filters in the two phase mode of operation unless expressly stated otherwise.

5. A four phase clock generator was to be included on chip. Provision was to be made for this clock generator to be disconnected from the circuit in order to permit the use of external clock pulses. The clock generator will be described in Section 7.10.

6. Two completely independent adaptors were to be
included on the IC. These adaptors were to have all their inputs and outputs available externally for testing purposes.

7. Two sample-and-hold circuits, one buffer and one operational amplifier were also to be included.

8. A test Switched-Capacitor structure of the type described in Section 2.2.2 was also to be included. No further reference will be made to this circuit as it was not part of this work.

7.2 THE FABRICATION PROCESS USED.

The IC was to be fabricated on a six micron double polysilicon gate, N channel, NMOS process by Plessey Research, (Caswell) Ltd. This process is reasonably typical of a large number of NMOS processes, and thus the detailed calculations given here pertaining to the prototype IC are broadly applicable to other processes. The design rules for the process used are given in appendix three. A double polysilicon gate process has five circuit layers available though not all are usable for any given circuit function. A cross-section of a section of circuit in which every layer is used in is given in Fig. 7.2.

7.3 COMPONENTS REQUIRED FOR THE DESIGN.

A wave filter of the type to be implemented here has three main types of components. These are switches, capacitors and buffers. These are all available in an NMOS process and each will be described separately in the
Figure 7-2: Cross-section of a chip built using a double polysilicon gate process, showing the five layers available. Following three subsections.

7.3.1 Switches.

A switch can be made from a single, minimum size, MOS enhancement transistor as shown in Fig. 7.3.

Figure 7-3: Equivalence between a switch and a minimum geometry NMOS transistor.
The use of a six micron process implies that the switch transistor, being of minimum size, has a channel length and width of six microns. The overall size of the transistor depends on the circuit layers to which it is connected but if, for example, it was connected to the aluminium layer on each side, the whole switching transistor would fit inside a rectangle with dimensions of 36 microns by 12 microns. This switching transistor is not identical to a perfect switch as it has a non-zero resistance when it is turned ON. The value of this resistance can be found as follows. From any MOS design reference book, for example [49], we can find that the ON resistance of a transistor, \( R_{on} \), is

\[
R_{on} = \left| \frac{\beta W}{\frac{W}{L} (V_g - V_t)} \right|^{-1}
\]

where \( \beta \) is the gain factor, \( \frac{W}{L} \) is the aspect ratio of the transistor, \( V_g \) is the voltage from the gate to the source of the transistor and \( V_t \) is the threshold voltage. In the Plessey process (see appendix three), \( \beta \) has a value of 25uA/V^2 and \( V_t \) has a maximum value of 1.25V for the P1 enhancement transistors used. The switching transistors used in these circuits are usually of minimum geometry and hence have an aspect ratio \( \frac{W}{L} \) of one. The value of \( V_g \) is variable as it depends on the signal being switched and it is assumed here that \( V_g = 15V \). Substitution of these values into equation (7.1) gives a value for \( R_{on} \) of 2909 ohms. However, as already mentioned, this value depends on the value of \( V_g \) and will generally be higher than the 2909 ohms.
calculated, and because of this we will assume a more conservative value of 5000 ohms. This resistance may seem to be high, but when it is remembered that the largest possible capacitor on an integrated circuit is of the order of 100pF, it can be seen that the $RC$ time constant is 0.5 micro-seconds. If the switch is ON for a time equivalent to ten $RC$ time constants we can be sure that virtually all charge transfer has taken place. If the clock pulse that turns the switch ON has a duty cycle of 33% the maximum clocking speed that can be used is 67kHz, adequate for the design target of 60kHz.

The OFF resistance of the MOST switch is many meg-ohms and the leakage current is so small that it can be neglected in the prototype. This is particularly so because the junction areas for a unity aspect ratio MOST are of minimum size. This should ensure good performance at high temperatures, bearing in mind the fact that leakage currents in silicon devices approximately double for each 10 degrees Kelvin rise in temperature [49].

The Plessey process rules (see Appendix 3) show that an enhancement transistor which uses the polysilicon level one for its gate has a threshold voltage of about one volt. This implies that the transistor switch will not turn ON unless the voltage on its gate exceeds the voltage on one of its other (drain/source) terminals by at least one volt. As the clock signals will have a logic '1' level of 15 volts, this limits our effective signal to a 14 volt maximum. In fact
this is not a limitation because the buffers used in the circuit will only amplify signals in the range 3.5 volts to 8.5 volts.

There are stray capacitances associated with a transistor switch and these are also shown in Fig. 7.3. The capacitors Cgs allow noise from the clock pulses to be superimposed on the signal. This is not a serious problem as the introduced noise signal is at a frequency above the Nyquist limit of the filter.

The capacitors Cd and Cs are of more significance. These contribute to the stray capacitances discussed in Section 5.2. More importantly they are voltage dependent capacitances and as such have the effect of increasing the non-linearity, and hence signal distortion, in the filter.

An IC layout of a switching MOS transistor with dimensions marked is given in Fig. 7.4. This is the smallest possible size for such a transistor when it is connected to aluminium tracks on each side, though, in some other cases, it is possible to reduce it still further. The diffusion is drawn with solid lines and all other levels are drawn with dotted lines. An important factor to be considered when using such a MOS transistor switch is the amount of stray capacitance it adds to the circuit. Any stray capacitance there may be comes from either the diffusion area to Substrate capacitance or the diffusion perimeter to Substrate capacitance. (See Appendix 3.)
Dimensions in microns.

Figure 7-4: Integrated circuit layout of a minimum geometry transistor switch.

The active area which makes up each side of the switch shown in Fig. 7.4 is 162 square microns. From the data given in appendix three it can be calculated that the capacitance this causes is

\[
Ca = \frac{162 \times 0.7}{(V + 0.6)^{1/2}} \times 10^{-4} \text{ pF} \tag{7.2}
\]

\[
= 113.4 \times 10^{-4} / (V + 0.6)^{1/2} \text{ pF}
\]

For an operating point of 10 volts this represents a capacitance of 0.0035pF.

The periphery term may be calculated similarly. The total periphery of the switch active area is 54 microns and the capacitance due to this periphery may be calculated from the information given in Appendix 3 as follows.
For an operating point of 10 volts this represents a capacitance of 0.02 pF.

The sum of these two capacitances gives the total stray capacitance on one side of this MOST switch. At an operating point of 10 volts the total stray capacitance will be 0.0235 pF. It should be noted that the periphery term, \( C_p \), is dominant.

In Fig. 7.5 the stray capacitance introduced by one side of a minimum geometry MOS switching transistor is graphed against the operating point of the switch in volts. The introduction of such voltage dependent capacitors is inevitable in any system which uses switching transistors. There is no way of avoiding this except the use of circuits which are "parasitic insensitive".

7.3.2 Capacitors.

Capacitors can be formed in any one of four ways in an integrated circuit which is to be fabricated by Plessey.

1. Polysilicon level one (Pi) to diffusion.

2. Polysilicon level two (P2) to diffusion.

3. Polysilicon level two to Polysilicon level one to diffusion. This results in two capacitors in series, a topmost plate on level P2, a middle
Figure 7-5: Graph of the stray capacitance present between one side of a transistor switch and Substrate, against the operating potential of the switch.
plate on level P1 and a lowermost plate on the diffusion.

4. Polysilicon level two to Polysilicon level one over field oxide.

Notice that the Plessey rules (see Appendix 3) do not permit the use of the aluminium level for the construction of capacitors.

Case two is very similar to case one with the exception that P2 is used instead of P1. It would be unusual to use P2 instead of P1 for such a capacitor as the process variations in the fabrication of the P2 level are much greater than those in the fabrication of the P1 level. This would lead to an unnecessary decrease in the accuracy of the capacitor values.

Polysilicon level one to diffusion capacitor.

A capacitor of the type P1 to diffusion is shown viewed from above in Fig. 7.6(a) and in cross-section in Fig. 7.6(b). It must be remembered that, in the Plessey process (see appendix three), the diffusion process takes place after the polysilicon levels have been laid down. 'This implies that the diffusion bottom plate of the capacitor will form a ring around the P1 top plate. It can be seen from Fig. 7.6(b) that the structure is similar to a MOS transistor when viewed in cross-section and, just as in a MOS transistor, charge will not be free to move under the P1 gate to form the bottom plate of the capacitor unless the
Figure 7-6: Integrated circuit layout of a P1 to diffusion capacitor.

Voltage between the P1 and the diffusion is greater than the threshold voltage. It is essential for normal operation of the capacitor that the threshold voltage is negative and therefore the complete capacitor is included within the depletion mask area. (Level 2.)

There is a very substantial voltage dependent stray capacitance between the diffusion or lower plate of the capacitor and the Substrate. It is vital that the circuit used is such that this bottom plate is always driven from a very low impedance voltage source, as only under those conditions is the stray capacitance unimportant.

There is also a stray capacitance between the P1 top plate and Substrate but it is very small indeed, as the P1 top plate is shielded from the Substrate by the bottom plate.

The capacitance of a P1 to diffusion capacitor is very
slightly voltage dependent \([50, 51]\). This effect was not realised until after the integrated circuit design was completed and it did contribute to the non-linearity of the circuit, as noted in section 8.4.2.

**P1 to P2 capacitor.**

A capacitor of this type is shown in Fig. 7.7.

![Figure 7-7: Integrated circuit layout of a P1 to P2 capacitor.](image)

It is the simplest and best type of capacitor to use in an integrated circuit design as it does not exhibit the voltage dependent effects of P1 to diffusion capacitors. It has, however, one major disadvantage: the polysilicon level two is poorly defined and hence the absolute value of the P1 to P2 capacitance is liable to variation. Even accurate capacitor ratios are difficult to achieve as the dimensions of a section of polysilicon level two will vary according to process parameters. Only two capacitors that are designed to have identical size and shape can be said to have an accurately defined ratio after process variations are taken into account. Ratios of capacitors of \(N\) to 1, where \(N\) is greater than about ten, can be achieved with some accuracy if one capacitor is formed from a single cell and the other
is formed from \( N \) of these cells, physically separate but connected in parallel [52]. This solution does, however, increase the stray capacitances present in the circuit.

There is a sizable stray capacitance from the P1 bottom plate of the capacitor to Substrate. For this reason, as for the P1 to diffusion capacitor, the bottom plate must always be driven from a voltage source.

**P1 to P2 to Diffusion. Two capacitors in series.**

This approach has both the good and the bad points of the two previously mentioned types. The P1 to P2 capacitor has a poorly defined value, while the P1 to diffusion capacitor is slightly voltage dependent. Using this technique does, however, give two capacitors in the layout area that would be occupied by only one capacitor if either of the other two methods were used. For this reason, and also because the adaptor cell requires two capacitors in series, this type of capacitor was used in the integrated circuit design.

7.3.3 Buffers.

The buffer amplifier required for this circuit was designed by Dr. Peter B. Denyer who at the time worked with Denyer Walmsley Microelectronics Ltd. For full details of its operation the reader is referred to [53], but a short description of the fairly conventional design will be given here for completeness.

The buffer was constructed from a conventional operational amplifier [54, 55, 56, 57] in voltage follower
mode, the target specification for which is given in Appendix four.

Consider an operational amplifier with open loop gain $A_o$ connected as a voltage follower. The gain, $A_b$, of the resulting buffer is given by

$$A_b = \frac{A}{1 + A_o}$$

(7.4)

Thus to achieve a buffer gain of $A_b$, where $A_b$ is in the range

$$1 - \frac{1}{e} < A_b < 1$$

(7.5)

we require

$$A_o > \frac{1}{e} - 1$$

(7.6)

Thus, to achieve a buffer gain of greater than 0.999 we require the open loop gain of the amplifier, $A_o$ to be such that

$$A_o > 1 / 0.001 - 1 = 999$$

(7.7)

Other requirements for the buffer were that it was to be capable of driving on-chip loads of up to 40pF, as the capacitors to be used in the circuit were to be about this size, and off-chip loads of up to 20pF. The buffer input capacitance was to be minimised, as this capacitance becomes part of the stray capacitances present in the circuit, and also to be minimised were the circuit layout area and power dissipation.

The final circuit employed 18 P1 gate enhancement transistors and 6 P2 gate depletion transistors, giving a total of 24 MOS transistors. The input capacitance was calculated to be 0.08pF and the overall layout area was
0.087mm$^2$. The output voltage swing of the buffer was 3.5 to 8.5 volts, limited by the fact that there are transistors within the buffer from its output to both the Vdd and Vss power supply rails and for the operational amplifier on which the buffer is based to achieve its full gain, these devices must be in saturation.

7.4 THE "ANALOGUE ZERO".

The circuit used for an adaptor is given in Fig. 7.8.

![Diagram](image)

**Figure 7-8:** The two-port adaptor circuit showing the 'analogue zero' connection.

The only difference between this circuit and the one previously shown as Fig. 5.3 is that the earth connection shown in Fig. 5.3 has been replaced by an "analogue zero" connection. In this IC design, which uses the buffers described in the last section, it is necessary to have all signals in the range 3.5 to 8.5 volts, as the buffer
amplifiers will only produce non-saturated outputs in this operating region, see Appendix four. This implies that the reference voltage which acts as the "zero" for the wave quantities in the filter should be midway between 3.5 and 8.5 volts. The filter therefore requires a steady voltage of about 6 volts to act as a level to which all signal voltages in the filter can be referenced. This reference voltage will be known as the analogue zero. The filter input and output signals will have a DC offset equal to the analogue zero level.

7.5 ADAPTOR LAYOUT.

It will be remembered that only the ratio of the capacitors shown in Fig. 7.8 as C1 and C2 must be accurately defined in the adaptor. If the effects of the circuit stray capacitances are ignored the absolute values of the capacitors CT1 and CT2 are not important. To achieve some degree of accuracy in the ratio of C1 to C2 it is necessary to make these capacitors in the same way on the IC and both C1 and C2 were made from P1 to diffusion capacitors which were ratioed by area directly; no attempt was made to use methods which could have given a higher degree of accuracy. Capacitors C1 and C2 were also positioned adjacent to each other to help to reduce the effects of process parameter variations across the IC.

The capacitors CT1 and CT2 were positioned in one of two ways, depending on the value of C2 and this is discussed further in the next two sections.
7.5.1 High values of C2.

When, in a particular design, the adaptor multiplier is required to be low, C2 must have a greater value than C1 and therefore C2 will occupy a fairly large layout area. In this case the capacitors CT1 and CT2 would be fabricated directly above C2. This adaptor layout implies that the layout area available for each of CT1 and CT2 is a little less than half that occupied by C2. Since the capacitance per square micron of a P2 to P1 capacitor is half that of a P1 to diffusion capacitor, (see Appendix 3) the capacitance of CT1 and CT2 is about one quarter that of C2. Only when the value of C2 was above about 15pF was this method used as only then were CT1 and CT2 each greater than 3.5pF, the minimum judged to be acceptable. The resulting adaptor layout is given in Fig. 7.9 and will be known as adaptor type one.

7.5.2 Low values of C2.

The method described above was perfectly acceptable if the value of C2 was fairly high, but if the adaptor multiplier had a value close to one, which resulted in a very small value for C2, placing CT1 and CT2 above C2 gave them unacceptably low values of capacitance. In this situation another layout, shown in Fig. 7.10, was used. As can be seen from the figure the capacitors CT1 and C2 are now physically separate in the layout.

We will now restrict our discussion to the CT1 capacitor but everything which applies to it also applies to the CT2
Adaptor type one, $Ad(3,1)$. 

Figure 7.9: Adaptor type one circuit layout.
Adaptor type two, Ad(3,2).

Figure 7.10: Adaptor type two circuit layout.
capacitor because of the symmetry of the circuit.

The CT1 capacitor is still made from the P2 to P1 levels, but now the side of the capacitor that gives the adaptor output, and is connected to the buffer, is the P1 plate. This would normally result in a very large stray capacitance from the P1 plate to Substrate. In this circuit, however, the output of the (already available) buffer amplifier which is at a voltage equal to that on the P1 capacitor plate, is connected to the diffusion plate under the P1 level. This ensures that the diffusion is always forced to be at the same voltage as the P1 plate. This gives a value for the effective stray capacitance equal to the normal capacitance divided by the open loop gain of the buffer. The CT1 capacitor was designed to have a capacitance of 5pF which would normally result in a stray capacitance of twice that value if the capacitor was fabricated over thin oxide, but because of the feedback connection from the buffer this stray, or undesirable, capacitance is reduced to an acceptable value of about \((10/5000)\)pF = 0.002pF. Adaptors which have the layout which results from this technique will be known as adaptor type two.

7.6 MIRROR-IMAGING OF ADAPTORS.

It has already been observed in section 5.7 that the value of the adaptor multiplier in a wave filter based on a symmetrical cascaded transmission line filter alternates between positive and negative values as the adaptor number increases. This statement can be expanded and put more
formally as in the following lemma; its proof is given as appendix five.

Lemma.

Consider a $N^{th}$ order cascaded transmission line filter which has the property that

$$R(N - i + 1) \ast R(i) = S \text{ for } N \text{ even}$$
$$R(N - i + 1) = R(i) \text{ for } N \text{ odd}$$

for all $i$, where $R(i)$ is the characteristic impedance of the $i^{th}$ section of transmission line.

When this reference filter is transformed into a wave filter using two-port adaptors the multipliers have the property that

$$(N - i + 2) = \alpha(i) \text{ for } N \text{ even, }$$  \hspace{1cm} (7,8)  $$

$$(N - i + 2) = -\alpha(i) \text{ for } N \text{ odd }$$

where $\alpha(i)$ is the multiplier of the $i^{th}$ adaptor.

In fact, if $N$ is odd or if the filter has a Butterworth response, $S=1$ and if $N$ is even $S$ is equal to the pass-band VSWR of a Chebyshev filter.

In the integrated circuit design under consideration the order of the filter is odd so there are an even number of adaptors and the adaptor multiplier values are mirror imaged and also negated. It would be possible to use this fact to advantage in the integrated circuit design if a simple method could be found to change the sign of the adaptor multipliers. It will now be shown that this can be achieved
simply by interchanging the ports of the adaptors; that is the port that was port one when the multiplier was positive becomes port two when the multiplier is negative and the port that was port two becomes port one in the adaptor with the negative multiplier.

Let us create some new dashed variables to represent the adaptor with its port interchanged.

Let \( A_1' = A_2, \quad A_2' = A_1, \quad B_1' = B_2, \quad B_2' = B_1 \), and \( \alpha' = -\alpha \).

Now \( B_1 = A_2 + \alpha(A_2 - A_1) \) from equations 3.24.

Substituting the dashed variables we have

\[
B_2' = A_1' - \alpha'(A_1' - A_2')
\]
\[
= A_1' + \alpha'(A_2' - A_1') \quad (7.9)
\]

Similarly

\( B_2 = A_1 + \alpha(A_2 - A_1) \) from equations 3.24.

Substituting the dashed variables we have

\[
B_1' = A_2' - \alpha'(A_1' - A_2')
\]
\[
= A_2' + \alpha'(A_2' - A_1') \quad (7.10)
\]

Using this result it can be seen that though in a seventh order filter, for example, there are eight adaptors, it is only necessary to design the first four adaptors as the second four are identical to these, the only difference lying in their method of interconnection.

7.7 ESTIMATION OF CIRCUIT STRAY CAPACITANCES.

Equation 5.17 shows that it is possible to adjust the ratio of \( C_1 \) to \( C_2 \) in order to compensate to some extent for the effects on the adaptor multipliers of the stray
capacitances present in the circuit. For this to be attempted it is necessary to estimate the values of the stray capacitances in the circuit from the layout and the process parameters given in Appendix three. Such an estimation cannot be achieved with a high degree of accuracy for three main reasons. Firstly the process parameters given in Appendix three are themselves only estimates, calculated from measurements taken of previous circuits, and are liable to change very significantly from one production run to the next. Secondly, the dimensions drawn in the circuit layout are liable to be different from those actually achieved on the integrated circuit. This is due to limitations in the photo-lithography and variations in the etching processes used in the fabrication of the circuit. Thirdly, non-uniformity in the diffusion processes used in the fabrication of the circuit cause variations in the dimensions of the diffusion layer and in its capacitance per square micron with respect to the voltage applied.

The voltage dependent nature of capacitances associated with the diffusion layer is another factor that must be taken into account. In order to estimate the size of such stray capacitances the voltages applied to them must be known. However, this voltage usually is variable and therefore it is required to fix a mean voltage about which it is hoped the capacitor will operate, and find the capacitance associated with this voltage level. This leads to further inaccuracies in the estimation of the stray
capacitances. In this circuit it was decided to assume an operating point equal to the analogue zero level (see section 7.4) for the capacitors, Since the Substrate is at -5 volts with respect to Vss, and the analogue zero level with respect to Vss is 6 volts, this represents an operating point of 11 volts for the stray capacitances. This implies that the capacitances associated with the diffusion layer are (from the design rules given in appendix 3)

$$\text{Area term} = \frac{0.7}{(11 + 0.6)} X 10^{-4} \text{ pF/um}^2$$

$$= 2.0553 \times 10^{-5} \text{ pF/um}^2 \quad (7.11)$$

$$\text{Perimeter term} = \frac{8}{(11 + 0.6)} X 10^{-4} \text{ pF/um}$$

$$= 3.534 \times 10^{-4} \text{ pF/um} \quad (7.12)$$

Using these two values, and the other information given in Appendix three, the following estimates of the stray capacitances present in the circuit have been made. In each case the area of a particular structure has been estimated from the IC layout.

7.7.1 Buffer amplifier input capacitance.

It is necessary to estimate the capacitance present at the input of the buffer amplifier as this will be a significant contribution to the stray capacitances CTS1 and CTS2. The capacitance is made up as follows:

<table>
<thead>
<tr>
<th>Cause</th>
<th>Area $\mu$m$^2$</th>
<th>Capacitance in pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1 over thin oxide</td>
<td>100</td>
<td>0.0360</td>
</tr>
</tbody>
</table>
P1 over field oxide 190 0.0068
Al over field oxide 684 0.0123
Al over Pi 240 0.0072
Al over P2 705 0.0233
Total 0.0856pF.

7.7.2 Stray capacitances CTS1 and CTS2 in adaptor type one.

These stray capacitances, which are equal in value because of a completely symmetrical circuit layout, are made up as follows.

<table>
<thead>
<tr>
<th>Area $\mu$m$^2$</th>
<th>Capacitance in pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion area</td>
<td>342</td>
</tr>
<tr>
<td>Diffusion perimeter ($\mu$m)</td>
<td>78</td>
</tr>
<tr>
<td>P2 over field oxide</td>
<td>282</td>
</tr>
<tr>
<td>Al over field oxide</td>
<td>30</td>
</tr>
<tr>
<td>P1 to channel ($\mu$m)</td>
<td>6</td>
</tr>
<tr>
<td>Buffer input capacitance</td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
</tr>
</tbody>
</table>

Therefore in adaptor type one $CTS_1 = CTS_2 = 0.1347pF$

7.7.3 Stray capacitances CTS1 and CTS2 in adaptor type two.

These stray capacitances, which are again equal because of a symmetrical circuit layout, are made up as follows.

<table>
<thead>
<tr>
<th>Cause</th>
<th>Area $\mu$m$^2$</th>
<th>Capacitance in pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1 over field oxide</td>
<td>138</td>
<td>0.0050</td>
</tr>
<tr>
<td>Diffusion area</td>
<td>342</td>
<td>0.0070</td>
</tr>
<tr>
<td>Diffusion perimeter ($\mu$m)</td>
<td>78</td>
<td>0.0276</td>
</tr>
<tr>
<td>P1 to channel ($\mu$m)</td>
<td>6</td>
<td>0.0027</td>
</tr>
<tr>
<td>Al over field oxide</td>
<td>131</td>
<td>0.0024</td>
</tr>
<tr>
<td>Buffer input capacitance</td>
<td></td>
<td>0.0856</td>
</tr>
</tbody>
</table>
Total \hspace{1cm} 0.1303 \text{pF}.

Therefore in adaptor type two \( CTS1 = CTS2 = 0.1303 \text{pF} \)

### 7.7.4 Stray capacitance \( CS1 \).

The value of this stray capacitance does not depend on whether the adaptor is of type one or two and is made up as follows.

<table>
<thead>
<tr>
<th>Cause</th>
<th>Area ( \mu m^2 )</th>
<th>Capacitance in ( \text{pF} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion area term</td>
<td>284</td>
<td>0.0058</td>
</tr>
<tr>
<td>Diffusion perimeter ((\mu m))</td>
<td>88</td>
<td>0.0311</td>
</tr>
<tr>
<td>( P1 ) over field oxide</td>
<td>120</td>
<td>0.0043</td>
</tr>
<tr>
<td>( P1 ) to channel ((\mu m))</td>
<td>12</td>
<td>0.0054</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>0.0466 \text{pF}</strong></td>
</tr>
</tbody>
</table>

Therefore \( CS1 = 0.0466 \text{pF} \) for both adaptor types.

It will be remembered that this stray capacitance is the most critical in the circuit and that its value must be minimised. The figures shown are for a layout using the best possible type of switch connections.

### 7.7.5 Stray capacitance \( CS2 \).

In the case of adaptor type one \( CS2 \), being identical in every way to \( CS1 \), has the same value as \( CS1 \). However in the case of adaptor type two this stray has a slightly larger capacitance due to the connection from the \( P1 \) level to \( P2 \) level that now has to be made. The stray capacitance in this case is made up as follows.

<table>
<thead>
<tr>
<th>Cause</th>
<th>Area ( \mu m^2 )</th>
<th>Capacitance in ( \text{pF} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion area term</td>
<td>284</td>
<td>0.0058</td>
</tr>
<tr>
<td>Diffusion perimeter ((\mu m))</td>
<td>88</td>
<td>0.0311</td>
</tr>
<tr>
<td>( P1 ) to channel ((\mu m))</td>
<td>12</td>
<td>0.0054</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Area</td>
<td>Value</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>P1 over field oxide</td>
<td>420</td>
<td>0.0151</td>
</tr>
<tr>
<td>A1 over field oxide</td>
<td>122</td>
<td>0.0022</td>
</tr>
<tr>
<td>P2 over thin oxide</td>
<td>60</td>
<td>0.0180</td>
</tr>
<tr>
<td>P2 over field oxide</td>
<td>508</td>
<td>0.0203</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>0.0979pF</strong></td>
</tr>
</tbody>
</table>

Therefore in adaptor type one CS2 = 0.0466pF
and in adaptor type two CS2 = 0.0979pF

7.8 FINAL CAPACITOR SIZES.

The capacitor values used in the integrated filters can be classified into two types: those which are common to all three filters and those which are particular to a certain one of the filters.

7.8.1 Capacitor values that are common to all three filters.

The size of the capacitor C1 was fixed at 30.037pF in all adaptors. The value actually aimed at was 30pF, chosen to be as big as possible to swamp the effects of the circuit stray capacitances but still be within the driving capabilities of the buffer amplifiers. Once the capacitor was laid out on the IC its area was calculated by using the information contained in the Plessey design rules (see appendix three) and was found to be 30.037pF. Rather than change the IC layout this value was accepted. In adaptor type one the size of CT1 and CT2 was 0.23 times that of C2. This figure was arrived at by noting that the capacitance per unit area of the P2 to P1 layer is one half that of the P1 to diffusion layer and that the area of the CT1 and CT2 capacitors was slightly less than half that of the C2
capacitor. This implied that the capacitance of the CT1 and CT2 capacitors had to be slightly less than one quarter of the capacitance of C2 and the figure was fixed at 0.23. In adaptors of type two capacitors CT1 and CT2 were fixed at 4.9876pF. These capacitor sizes are all very large but this was a prototype circuit and no redesigns were possible so it was decided to be very conservative in the choice of capacitor values.

The sizes of C2 were fixed according to whether the adaptor was of type one or two and according to equation 5.17, which is reproduced below.

\[
\alpha' = \frac{C1 \times CT}{CTS + CT / (C1 + C2 + CS1 + CS2 + \frac{2 \times CTS \times CT}{CTS + CT})}
\]

For adaptor type one CT = 0.23 * C2. This results in the above equation becoming a quadratic in C2 which can be written as follows.

\[aC2^2 + bC2 + c = 0\]

where \(a = 0.23 \times \alpha\)

\[b = 0.23(\alpha C1 + \alpha CS1 - C1 + \alpha CS2 + 2\alpha CTS) + \alpha CTS,\]

and \(c = \alpha CTS(C1 + CS1 + CS2)\)

Adaptors of type one were used for the first adaptor (and therefore for the last adaptor, see Appendix five) of all the filters to be designed.

For adaptors of type two CT is fixed at 4.9876pF. This gives a linear equation for C2 which can be written as follows:
In the design of the adaptors of type two an unaccountable error was made. The value of CTS was taken to be 0.18889pF rather than the correct value of 0.1303pF. This has resulted in the capacitor sizes actually used for C2 being lower than they should have been, which has given multipliers which are about 1.5% too high.

7.8.2 Capacitor values that are particular to a certain filter.

In the immediately preceding section the equations and capacitor values that are common to all three integrated filters were described. In this section the capacitor values that are particular to each of the filters fabricated are given, together with the effect on the adaptor multipliers of the error made in the calculation of CTS.

Let \( \text{Ad}(N,M) \) mean the \( M^{\text{th}} \) adaptor of the \( N^{\text{th}} \) order filter and let \( R(N,M) \) be the characteristic impedance of the \( M^{\text{th}} \) section of line in the \( N^{\text{th}} \) order filter. Then \( N = 3, 5 \) or 7, and \( M \) is in the range 1 to \( N+1 \) for the adaptors, and in the range 1 to \( N \) for the transmission lines.

The characteristic impedances of the transmission line sections that make up the reference filters were taken from tables, [17] the relevant sections of which are summarised in Table 7.1.

Let \( \alpha(N,M) \) be the multiplier of the \( M^{\text{th}} \) adaptor in the

\[
\begin{align*}
C_2 &= \frac{C_1 \ast CT}{\alpha(CTS + CT)} - \frac{(C_1 + CS_1 + CS_2) \ast 2 \ast CTS \ast CT}{CTS + CT}
\end{align*}
\]
Table 7-1: Characteristic impedances of the sections of transmission line that make up the reference filters.

\[
\alpha(N,M) = \frac{R(N,M-1) - R(N,M)}{R(N,M-1) + R(N,M)} \quad (7.15)
\]

This gives the values for the adaptor multipliers set out in Table 7.2.

When these values of \( \alpha \) are substituted into equation 7.13
for adaptors of type one, or into equation 7.14 for adaptors of type two, the values for C2 are as given in Table 7.3, where C2(N, M) is the C2 value for the Mth adaptor in the filter of order N.

<table>
<thead>
<tr>
<th>C2(N, M) pF</th>
<th>3</th>
<th>5</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>27.0749</td>
<td>23.2828</td>
<td>22.2301</td>
</tr>
<tr>
<td>2</td>
<td>6.7541</td>
<td>4.5947</td>
<td>4.2190</td>
</tr>
<tr>
<td>3</td>
<td>6.7541</td>
<td>2.4407</td>
<td>2.0965</td>
</tr>
<tr>
<td>4</td>
<td>27.0749</td>
<td>2.4407</td>
<td>1.7534</td>
</tr>
<tr>
<td>5</td>
<td>-</td>
<td>4.5947</td>
<td>1.7534</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td>23.2828</td>
<td>2.0965</td>
</tr>
<tr>
<td>7</td>
<td>-</td>
<td>-</td>
<td>4.2190</td>
</tr>
<tr>
<td>8</td>
<td>-</td>
<td>-</td>
<td>22.2301</td>
</tr>
</tbody>
</table>

Table 7.3: Calculated C2 capacitor values.

Table 7.3 gives the correct values for the capacitors C2. However, due to an error in the calculation of the stray capacitance CTS, the values actually used in the three filters were slightly different and are as given in Table 7.4. The use of these values of C2 resulted in the multipliers of the type two adaptors being 1.5% high, which would clearly lead to a difference between the experimental results and the desired response.

7.9 DESIGN TOOLS.

The integrated circuit was designed using the so-called GAELIC suite of computer programs on the Edinburgh DEC System 10 [58]. This integrated circuit design aid was originally developed at Edinburgh University and was then
taken over by Compeda Ltd, who have continued its
development and now market GAELIC to other companies who
design integrated circuits.

The versions of GAELIC available at the time of this
circuit design were "original" GAELIC and Revision 10, which
were rather inefficient in their use of computer time
compared to the Revision 12 now available. The original
version of GAELIC was the one actually used because the
post-processor, that is the program which translates the
data output from GAELIC into a form compatible with the-mask
making machine, was not available for Revision 10. Because
of this some of the features of GAELIC could not be used as
it was found that they had unexpected side-effects in this
early version. However, despite this the original version
of GAELIC was very usable and it is recognised that without
it this integrated circuit design would not have been

<table>
<thead>
<tr>
<th>M</th>
<th>27.0749</th>
<th>1.9517</th>
<th>1.2723</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>-</td>
<td>4.0814</td>
<td>1.2723</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td>23.2828</td>
<td>1.6114</td>
</tr>
<tr>
<td>7</td>
<td>-</td>
<td>-</td>
<td>3.7099</td>
</tr>
<tr>
<td>8</td>
<td>-</td>
<td>-</td>
<td>22.2301</td>
</tr>
</tbody>
</table>

Table 7-4: Values for C2 actually used.
possible.

7.10 CLOCK GENERATOR

An on-chip clock generator producing four phase non-overlapping clock pulses with a maximum frequency of 60kHz was designed on the integrated circuit. The output clock waveforms had to have a logic zero level of less than 0.5 volts, a logic one level of greater than 14.5 volts and had to be capable of driving capacitive loads of up to 7 pF. The outputs of the clock generator were to be switched to permit their complete disconnection from the circuit to allow external clock pulses to be applied to the filter. The input to the clock generator was to be a single-phase TTL and CMOS compatible clock waveform.

The clock generator was comprised of three main parts.

1. An input flip-flop to give antiphase clocks from the single phase input clock waveform.

2. A four stage shift register which included NOR gates present to ensure that output clock pulses could not overlap and also output switches to allow the clock generator to be completely disconnected from the filter circuit.

3. A three input NOR gate which fed back to the shift register input a logic one when the first three stages of the shift register contained only logic zeros.
These parts will be dealt with separately in the following subsections. In the MOS transistor circuits which will be shown only two of the four different types of transistor are used. All enhancement transistors have polysilicon one gates while all depletion transistors have polysilicon two gates. The transistor aspect ratios are shown in the figures alongside the transistors to which they refer.

7.10.1 Flip-flop.

A conventional cross-coupled NOR gate circuit was used for this flip-flop, as is shown in Fig. 7.11(a) which is drawn using logic symbols. Fig. 7.11(b) shows the same circuit made up from NMOS transistors. The threshold voltage of the input enhancement P1 transistor is 1 volt so the clock input is TT1 and CMOS compatible, as required.

7.10.2 Shift register cell.

The shift register is clocked by the CLK and CLK signals from the flip-flop described above. The circuit of a single cell of the shift register showing the switched output and the NOR gate which is present to prevent output clock pulses from overlapping, is given in Fig. 7.12(a) drawn in logic gate symbols, and in Fig. 7.12(b) drawn as a NMOS transistor circuit.

The shift register is conventional except that a NOR gate is used where there would normally be an inverter. The inclusion of this feature ensures that the output clock pulses cannot overlap, as the NOR gate prevents the Øn
Figure 7-11: The flip-flop which is used as the first section of the clock generator.
Figure 7-12: One cell of the four required to make the shift register used for the clock generator, showing the output switch and the NOR gate which is present to ensure that clock pulses cannot overlap.

output pulse from rising until the $\Omega_{n-1}$ output pulse has fallen below one volt. The output switch shown is a large depletion transistor, chosen as such to ensure that no voltage is dropped across it when it is turned ON. Had there been such a voltage the maximum available voltage of the logic one pulse available to the rest of the circuit would have been lowered below the 14.5 volts required. One consequence of this choice of transistor is that the transistor gate must be connected to the Substrate voltage ($-5$ volts) to turn the clock generator off.

7.10.3 Feed-back 3-input NOR gate.

The 3-input NOR gate used as the shift register feed-back is completely conventional and only serves to enter a logic
one into the input of the shift register when the first three registers are all at logic zero. This ensures that one, and only one, of the shift register outputs is at a logic one at any one time. This circuit also has the advantage that it is self-starting, i.e. no matter what conditions exist in the shift register at switch on the correct state will be entered into automatically.

7.10.4 SPICE simulation.

The complete clock generator circuit was simulated using the circuit simulation program SPICE [59] available on the Edinburgh DEC system 10 computer and the results are shown in Fig. 7.13. It can be seen from the figure that the specifications are met.

7.11 COMPLETE INTEGRATED CIRCUIT LAYOUT.

There are a total of 18 adaptors in the three filters designed, and they were laid out in three blocks of six, with adaptors which had positive multiplier values laid out as designed, and those with negative multipliers laid out mirror imaged to cause the ports to be interchanged as described in section 7.6.

A simplified block diagram of the integrated circuit is given in Fig. 7.14 and shows how the rectangular chip is broken into the three filter sections and the test structures. A micro-photograph of the corresponding circuit is given in Fig. 7.15. The adaptor structures can clearly be seen, as can the mirror imaging required to give the negative multiplier values. The overall chip size was 5 by 6
Figure 7-13: SPICE simulation results for the clock generator.
Figure 7-14: Simplified layout diagram of the integrated circuit.
Figure 7-15: Micro-photograph of the integrated circuit.
millimetres, though this figure could have been slightly reduced if the available space had been utilised more efficiently.