Figure 4-4: Three Transistor Dynamic RAM Layout (a).
Figure 4-5: Three Transistor Dynamic RAM Layout (b).
Figure 4-7: Six Transistor Static RAM Layout (a).
Figure 4–10: Five Transistor Static RAM Layout.
Figure 4–16: Pass Transistor Multiplexor Layout.
Figure 5-6: Plot of CLA Cell Before Personalisation.
Figure 5-8: Function Tiles.
Figure 5–9: Routing Tiles.
5.3 Wafer Scale Version.

This section will consider methods of mapping the dynamically programmable version of the architecture into Wafer Scale Integrations (WSI). There are several reasons for looking at wafer scale version of the CAL system. First, the design will require less area and power consumption due to the reduced size of the WSI. A design with a lower cost per chip will be more competitive in the market. Secondly, because there is only a single pattern of VLSI and wafers costs are identical, the wafer scale approach should result in lower wafer costs per chip.

Figure 5-10: Function Block Stage Layout.