COMMUNICATIONS FREQUENCY SYNTHESISERS
BASED ON
SURFACE ACOUSTIC WAVE OSCILLATORS

by

Kassim Muhawi Hussain B.Sc. (E.Eng.)

A thesis submitted to the Faculty of Science of the
University of Edinburgh, for the degree of
Doctor of Philosophy

Department of Electrical Engineering
July 1978
Surface Acoustic Wave (SAW)-controlled oscillators possess many features which make them attractive as frequency sources in communications applications. This thesis deals with SAW oscillators, both resonator and delay stabilised, and their incorporation in communications synthesiser modules intended primarily for mobile radio applications.

A review of SAW technology and the theory and design of SAW controlled oscillators together with related topics on frequency synthesis techniques is included. A SAW resonator-based personal radio-telephone module is described. This module demonstrates improved performance over existing commercial equipment. VHF and UHF multi-channel digital frequency synthesisers in which SAW delay line oscillators were successfully employed as frequency sources are also presented. Finally, a SAW based UHF Gemini synthesiser is demonstrated. This module is capable of fast switching, a feature of particular interest in frequency-hopped communications. All these modules are designed using the indirect frequency synthesis approach, in which the medium and long term stabilities of the SAW oscillators are controlled by a highly stable crystal reference.
Acknowledgements

I would like to express my sincere gratitude to Professor J H Collins, Dr P M Grant and Dr J H Hannah for their supervision and kind help, without which this work would not have reached this level.

I gratefully acknowledge the financial support of the Iraqi Government (Ministry of Defence).

Sincere thanks are due to many members of staff in the Department and friends, particularly; Mr R C Corner, Mr J T M Stevenson, Dr J Filshie, Mr E W Patterson, Mr M A Sharif, Mr W Hillam, Dr M A Jack and Mr C H C Matthews, whose assistance helped towards the completion of this thesis. Also I thank Mrs Ruth Gosden for typing the manuscript in a good presentable form.

Finally, I wish to express my gratitude to my father and brothers for their moral and material support. Also my appreciation to my wife for her patience.
| CONTENTS |
|-----------------|------|
| TITLE PAGE      | (i)  |
| ABSTRACT        | (ii) |
| DECLARATION OF ORIGINALITY | (iii) |
| ACKNOWLEDGEMENTS | (iv)  |
| CONTENTS        | (v)  |
| ABBREVIATIONS   | (vi) |

<table>
<thead>
<tr>
<th>CHAPTER I : Introduction</th>
<th>Page No</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CHAPTER II : Introduction to Surface Acoustic Wave Devices and their Capabilities</th>
<th>Page No</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 Introduction</td>
<td>5</td>
</tr>
<tr>
<td>2.2 Materials for SAW Devices</td>
<td>7</td>
</tr>
<tr>
<td>2.3 The Interdigital Transducer (IDT)</td>
<td>10</td>
</tr>
<tr>
<td>2.4 SAW Delay Lines</td>
<td>12</td>
</tr>
<tr>
<td>2.5 SAW Filters</td>
<td>14</td>
</tr>
<tr>
<td>2.6 SAW Devices and Applications</td>
<td>18</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CHAPTER III : Frequency Sources</th>
<th>Page No</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 Introduction</td>
<td>20</td>
</tr>
<tr>
<td>3.2 General Form of Oscillator Circuit</td>
<td>22</td>
</tr>
<tr>
<td>3.3 LC and Crystal Oscillators</td>
<td>23</td>
</tr>
<tr>
<td>3.4 SAW Delay Line Stabilised Oscillators</td>
<td>26</td>
</tr>
<tr>
<td>3.4.1 Basic Theory</td>
<td>26</td>
</tr>
<tr>
<td>3.4.2 The Quality Factor</td>
<td>28</td>
</tr>
<tr>
<td>3.4.3 Mode Selection</td>
<td>29</td>
</tr>
<tr>
<td>3.4.4 Frequency Modulation</td>
<td>31</td>
</tr>
</tbody>
</table>

Note: The Figures and Tables are included at the end of each section.
<table>
<thead>
<tr>
<th>Chapter</th>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>3.5.1</td>
<td>The SAW Resonator</td>
<td>33</td>
</tr>
<tr>
<td></td>
<td>3.5.2</td>
<td>The Surface Wave Cavity</td>
<td>34</td>
</tr>
<tr>
<td></td>
<td>3.5.3</td>
<td>A SAW Resonator Equivalent Circuit</td>
<td>36</td>
</tr>
<tr>
<td>3.6</td>
<td>3.6.1</td>
<td>Definition</td>
<td>39</td>
</tr>
<tr>
<td></td>
<td>3.6.2</td>
<td>Frequency Stability of LC and Crystal Oscillators</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td>3.6.3</td>
<td>Frequency Stability of SAW Oscillators</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CHAPTER IV</td>
<td>Frequency Synthesis</td>
<td>48</td>
<td></td>
</tr>
<tr>
<td>4.1</td>
<td></td>
<td>Introduction</td>
<td>48</td>
</tr>
<tr>
<td>4.2</td>
<td></td>
<td>Direct and Indirect Frequency Synthesisers</td>
<td>50</td>
</tr>
<tr>
<td>4.3</td>
<td>4.3.1</td>
<td>The Phase-Locked Loop (PLL)</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PLL Basic Configuration</td>
<td>53</td>
</tr>
<tr>
<td></td>
<td>4.3.2</td>
<td>The Digital PLL</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>4.3.3</td>
<td>Type and Order of the PLL</td>
<td>56</td>
</tr>
<tr>
<td></td>
<td>4.3.4</td>
<td>PLL Design</td>
<td>57</td>
</tr>
<tr>
<td>4.4</td>
<td></td>
<td>VHF/UHF Synthesiser Requirements</td>
<td>61</td>
</tr>
<tr>
<td>4.4.1</td>
<td></td>
<td>The Programmable Divider</td>
<td>61</td>
</tr>
<tr>
<td>4.4.2</td>
<td></td>
<td>Prescaling</td>
<td>62</td>
</tr>
<tr>
<td>4.4.3</td>
<td></td>
<td>Division Radix Requirements</td>
<td>67</td>
</tr>
<tr>
<td>4.4.4</td>
<td></td>
<td>Side-Step Requirements</td>
<td>68</td>
</tr>
<tr>
<td>4.5</td>
<td></td>
<td>The 'Gemini' Synthesiser</td>
<td>70</td>
</tr>
<tr>
<td>4.6</td>
<td></td>
<td>Phase-Noise Performance of Frequency Synthesisers</td>
<td>72</td>
</tr>
<tr>
<td>4.7</td>
<td></td>
<td>SAW Approaches to Frequency Synthesis</td>
<td>74</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CHAPTER V</td>
<td>Design and Performance of SAW Resonator Based</td>
<td>79</td>
<td></td>
</tr>
<tr>
<td>5.1</td>
<td></td>
<td>Introduction</td>
<td>79</td>
</tr>
<tr>
<td>5.2</td>
<td></td>
<td>The Synthesiser Module</td>
<td>80</td>
</tr>
<tr>
<td>Section</td>
<td>Title</td>
<td>Page</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>------------------------------------------------------------------------</td>
<td>------</td>
<td></td>
</tr>
<tr>
<td>5.3</td>
<td>SAW Resonator - Design and Performance</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td>5.3.1</td>
<td>Design Parameters</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td>5.3.2</td>
<td>Production</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td>5.3.3</td>
<td>SAW Resonator Measurements and Results</td>
<td>85</td>
<td></td>
</tr>
<tr>
<td>5.4</td>
<td>SAW Resonator Stabilised Oscillator</td>
<td>89</td>
<td></td>
</tr>
<tr>
<td>5.5</td>
<td>Phase-Locked Sampler and Loop Filter</td>
<td>91</td>
<td></td>
</tr>
<tr>
<td>5.6</td>
<td>Power Amplifier</td>
<td>94</td>
<td></td>
</tr>
<tr>
<td>5.7</td>
<td>Module Performance</td>
<td>95</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>CHAPTER VI</strong>: Design, Construction and Performance of Voltage-</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Controlled SAW Delay Line Oscillators</td>
<td>96</td>
<td></td>
</tr>
<tr>
<td>6.1</td>
<td>Delay Line Measurements</td>
<td>96</td>
<td></td>
</tr>
<tr>
<td>6.2</td>
<td>120 MHz SAW Delay Line Oscillator</td>
<td>99</td>
<td></td>
</tr>
<tr>
<td>6.2.1</td>
<td>Oscillator Design and Construction</td>
<td>99</td>
<td></td>
</tr>
<tr>
<td>6.2.2</td>
<td>Oscillator Performance</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>6.3</td>
<td>480 MHz DL SAW Oscillator</td>
<td>104</td>
<td></td>
</tr>
<tr>
<td>6.3.1</td>
<td>Oscillator Design and Construction</td>
<td>104</td>
<td></td>
</tr>
<tr>
<td>6.3.2</td>
<td>Oscillator Performance</td>
<td>104</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>CHAPTER VII</strong>: Design, Construction and Performance of SAW-</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Based Digitally Controlled Multi-Channel</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Synthesisers, for Mobile Radio Applications</td>
<td>108</td>
<td></td>
</tr>
<tr>
<td>7.1</td>
<td>Introduction</td>
<td>108</td>
<td></td>
</tr>
<tr>
<td>7.2</td>
<td>SAW Based VHF Digital Synthesiser</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>7.2.1</td>
<td>Synthesiser Design</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>7.2.2</td>
<td>The Programmable Divider</td>
<td>111</td>
<td></td>
</tr>
<tr>
<td>7.2.3</td>
<td>Fixed Dividers</td>
<td>112</td>
<td></td>
</tr>
<tr>
<td>7.2.4</td>
<td>Phase-Comparator, Loop Filter and Error Amplifier</td>
<td>114</td>
<td></td>
</tr>
<tr>
<td>7.2.5</td>
<td>Synthesiser Performance</td>
<td>120</td>
<td></td>
</tr>
</tbody>
</table>
7.3 SAW Based UHF Digital Synthesiser

7.3.1 Synthesiser Design 122
7.3.2 Dual-Modulus Preselector and Buffer Amplifier 123
7.3.3 Programmable Divider 124
7.3.4 Reference Divider 124
7.3.5 Phase-Comparator, Loop Filter and Error Amplifier 126
7.3.6 UHF Synthesiser Performance 127

7.4 SAW-Based UHF 'Gemini' Synthesiser 129

7.4.1 System's Design and Construction 129
7.4.2 Bandpass Filter and Mixer 132
7.4.3 Gemini Loop Performance 135

7.5 Summary 137

CHAPTER VIII Conclusion 138

REFERENCES 142

APPENDIX I : A Programme for the 112.7 MHz Resonator Mask

APPENDIX II : A Letter and a Publication Related to the Author's Work
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADF</td>
<td>Automatic Direction Finder</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>BPF</td>
<td>Bandpass Filter</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semi-conductor</td>
</tr>
<tr>
<td>DL-SAWO</td>
<td>Surface Acoustic Wave Delay Line Stabilised Oscillator</td>
</tr>
<tr>
<td>ECM</td>
<td>Electronic Counter Measure</td>
</tr>
<tr>
<td>ECL</td>
<td>Emitter-Coupled Logic</td>
</tr>
<tr>
<td>EM</td>
<td>Electro-Magnetic</td>
</tr>
<tr>
<td>FET</td>
<td>Field-Effect Transistor</td>
</tr>
<tr>
<td>FM</td>
<td>Frequency Modulation</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>IDT</td>
<td>Interdigital Transducer</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PCF</td>
<td>Pulse Compression Filter</td>
</tr>
<tr>
<td>PD</td>
<td>Phase Detector</td>
</tr>
<tr>
<td>PPM</td>
<td>Part Per Million</td>
</tr>
<tr>
<td>PRR</td>
<td>Pulse Repetition Rate</td>
</tr>
<tr>
<td>Q</td>
<td>Quality Factor</td>
</tr>
<tr>
<td>Q_U</td>
<td>Unloaded Q</td>
</tr>
<tr>
<td>Q_L</td>
<td>Loaded Q</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RAC</td>
<td>Reflective Array Compressor</td>
</tr>
<tr>
<td>SAW</td>
<td>Surface Acoustic Wave</td>
</tr>
<tr>
<td>SAWO</td>
<td>Surface Acoustic Wave Oscillator</td>
</tr>
<tr>
<td>SSBW</td>
<td>Surface Skimming Bulk Wave</td>
</tr>
<tr>
<td>SSB</td>
<td>Single Side Band</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>TB</td>
<td>Time-Bandwidth Product</td>
</tr>
<tr>
<td>$T_x/R_x$</td>
<td>Transmit/Receive</td>
</tr>
<tr>
<td>TTL</td>
<td>Transistor-Transistor Logic</td>
</tr>
<tr>
<td>UHF</td>
<td>Ultra High Frequency</td>
</tr>
<tr>
<td>VHF</td>
<td>Very High Frequency</td>
</tr>
</tbody>
</table>
To my children:

Nerjis, Yasmeen and Muhammed
CHAPTER I

INTRODUCTION

Radio traffic in the VHF/UHF frequency bands is increasing very rapidly with the requirement for large numbers of channels in a given band. This necessitates closer channel spacing, improved frequency stability and possibly faster channel selection. To meet these requirements, frequency synthesisers are now widely in use as transmitter exciters and receiver local oscillators in communications applications. These are capable of generating several closely spaced radio channels by controlling a tunable frequency source, normally a LC-VCO, through a phase-locked loop. However, in these communications synthesisers as the channel spacing is reduced to increase the number of available channels, the noise caused by adjacent channel interference can be a serious problem. To overcome this effect, oscillators with improved 'phase-noise' characteristics are required. The performance of LC-oscillators is limited by their instability and the practical Q values obtainable. Surface acoustic wave (SAW) delay line oscillators (DL-SAWO) possess the attractive features of high frequency stability and wide bandwidth FM deviation. This permits a single DL-SAWO to cover several radio channels and still have a sufficiently high Q to give satisfactory adjacent channel suppression. SAW oscillators are also rugged, compact and almost immune to mechanical shocks and vibrations, features of particular importance for communication synthesisers used in mobile radio applications.

Existing personal UHF radio-telephone designs are based on bulk crystal oscillators, the frequency of which is multiplied to obtain the required carrier signal. This multiplication process is a source
of additive noise at the output. SAW resonator controlled oscillators can operate fundamentally at UHF frequencies and therefore can be employed in personal radio-telephones eliminating the need for multipliers and providing considerably improved phase-noise performance and rf/dc efficiency.

Both delay line and resonator stabilised SAW oscillators can be designed with satisfactory short-term frequency stability, which is $Q$ dependent. Their medium and long-term stabilities are substrate material related and unless current research activity leads to a new very stable SAW material, are likely to remain inferior to the best bulk quartz crystal oscillators. However, these stability effects can be compensated for by phase-locking the SAW oscillator to a crystal reference. SAW oscillators and their application in phase-locked communication synthesisers are investigated in this thesis.

SAW technology, being the basis for this work, is introduced in Chapter 2. Emphasis is placed on related subjects such as SAW delay lines and SAW filtering characteristics together with a brief updated survey on SAW devices and their applications.

A study on various frequency sources is presented in Chapter 3, where crystal controlled and LC oscillators, which are the current signal sources in VHF/UHF communications systems, are first introduced. This is followed by a discussion on the DL-SAWO. Its fundamental theory, FM capability and mode selection are covered in detail. SAW resonators are then discussed with an emphasis on surface wave cavity requirements and resonator equivalent circuit. This chapter concludes with a section on the frequency stability of various frequency sources.

Chapter 4 deals with frequency synthesis techniques. Both
'direct' and 'indirect' synthesisers are discussed with emphasis being placed on the indirect technique due to its advantages. Phase locked loops (PLL) which form the basis for indirect synthesis are also covered. The design requirements for practical VHF/UHF frequency synthesisers are then explained in detail. Finally the synthesis approach introduced in this thesis is compared with other types of SAW based frequency synthesisers.

In Chapter 5, the design of a 112 MHz SAW resonator device is reported. This device was used as a frequency controlling element in a single transistor oscillator. The oscillator circuit design, which incorporates varactor phase-shifting networks to achieve FM capability, is described and its performance is presented. The design and performance of a single channel radio-telephone synthesiser module using a phase-lock approach are also presented.

In Chapter 6, consideration is given to the design and performance of two delay line stabilised oscillators, one operating at 120 MHz and the other at 460 MHz. The circuit design of each was optimised for the particular operating frequency and they were provided with phase-shifting networks enabling them to cover the maximum possible FM bandwidth for use in frequency synthesis applications.

Chapter 7 presents the design and performance of the first digitally-controlled multi-channel SAW based synthesisers operating at VHF and UHF frequencies. The controlled oscillators employed in these synthesisers were the SAW oscillators described in Chapter 6. These synthesisers were intended for mobile-radio communication. Hence, power dissipation, channel spacing, switching time between operating channels and FM capability were important design factors. The synthesisers were realized with different PLL design approaches.
Chapter 8 summarises important aspects of this research and includes suggestions for further applications of SAW oscillators in frequency synthesis.
CHAPTER II

INTRODUCTION TO SURFACE ACOUSTIC WAVE DEVICES
AND THEIR CAPABILITIES

2.1 INTRODUCTION

Surface Acoustic Waves (SAW) have attracted considerable attention in recent years for applications in electronics. However, their history goes back to 1885 when they were first discussed by Lord Rayleigh. Surface acoustic waves propagate with a velocity approximately $10^5$ times smaller than the electromagnetic (EM) wave velocity and their losses per wavelength of propagation are much smaller than that of guided EM waves. They propagate along the surface with mechanical displacements of amplitude decaying to negligible values in a depth of about a wavelength below the surface. In piezoelectric materials, this mechanical motion will be accompanied by an electric field of periodic nature outside the surface. This feature was exploited by White and Voltmer [1] in 1965 by introducing the interdigital transducer (IDT) that can be coupled piezoelectrically to the propagating wave.

Unlike the bulk acoustic waves, surface acoustic waves are continuously accessible throughout the propagation path, so it is possible to sample the wave, modify it and interact with it while it is propagating.

The IDT provides a convenient method for transduction of electrical to acoustic energy and simultaneously enables the
inherent versatility of SAW to be exploited. This gives surface waves great application potential in electronic and signal processing [2]. The IDT, complemented by low propagation loss piezoelectric materials, enables device conversion losses to be low up to 1 GHz. Collins, J H et al [3] reported in 1968 the first low loss (10 dB) VHF SAW delay line. Since 1967-68, there has been a growing interest in SAW technology. SAW devices have reached a point where advanced mathematical models are employed in their design and development [4] and they have proven to be valuable for a wide range of electronic systems [5]. Some of them are now operating in practical equipment, where they offer improvements in performance, size and cost [6]. The capabilities of SAW devices in signal processing [7, 8, 9] and communications [10, 11] are currently under investigation.
2.2 MATERIALS FOR SAW DEVICES

Crystalline materials with their low acoustic losses are of particular interest for SAW devices. The choice of material depends on the type of device required, time delay, operating frequency and system application. Important factors which should be considered in the material choice are: SAW velocity, piezoelectric coupling constant $K^2$, beam steering and diffraction, temperature sensitivity, propagation attenuation and non-linearity effect. These factors are defined below:

i) SAW Velocity: has direct relation to the time delay ($\tau$) of the SAW delay line path ($l$), $\tau = l/v$. To achieve very long delay, materials with slow velocity such as $\text{Bi}_{12}\text{GeO}_2$ and $\text{Tl}_3\text{TaSe}_4$ are convenient and should be considered to minimise the device size. On the other hand, the wavelength ($\lambda$), and hence the IDT finger width (see Section 2.3) is related to the frequency by $\lambda = v/f$ and therefore high velocity materials such as $\text{AlN/Al}_2\text{O}_3$ are required for high frequency applications to minimise the IDT fingers resolution and reduce fabrication difficulties.

ii) Piezoelectric coupling constant ($K^2$): is a measure of materials coupling efficiency. Materials with high $K^2$ give good conversion efficiency and wide bandwidth. $\text{LiNbO}_3$ is the best available material for large $K^2$ and hence for wide bandwidth applications.

iii) Beam steering and diffraction: secondary effects which are a source of additional losses and performance degrading. In practice, accurate alignment of the IDT together with proper material orientation can actively reduce these effects.
iv) Temperature sensitivity: is an important factor in determining the stability of SAW delay lines centre frequency against temperature variations. This factor is normally measured by the first order temperature coefficient of time delay, which is given by the difference between the first-order thermal expansion coefficient $1/\alpha \cdot \frac{d\alpha}{dT}$ and the first order temperature coefficient of surface wave velocity $1/\nu \cdot \frac{d\nu}{dT}$ [13] where $T$ is temperature. Temperature compensated materials are those for which this difference is equal to zero.

v) Propagation attenuation: the attenuation coefficient for SAW is proportional to the square of the operating frequency for most crystalline materials, and for the majority of SAW materials the wave attenuation can be neglected in the VHF/UHF region, but should be considered as the frequency goes higher [14].

vi) Non-linearity effect: this factor reduces the practical power handling capability of SAW devices. It is frequency related and is a source of additional losses and generation of harmonics [14]. In high frequency applications it limits the dynamic range of the devices.

Presently, the most common materials in use for SAW devices are Quartz and Lithium-niobate. ST-quartz has a very low temperature coefficient of delay and for this reason it is mainly used for applications requiring good frequency stability. However, it has a small coupling constant which limits its available bandwidth. On the other hand, Lithium-niobate has a very large coupling constant, an essential factor for large bandwidth low loss devices [13], but its temperature sensitivity is large and a means of temperature control is required. Considerable work has recently been
directed towards the realization of substrate materials with zero temperature sensitivity and high coupling constant. This search has succeeded in finding materials which are better than ST-quartz. Among these is an SiO$_2$/LiTaO$_3$ composite structure, which is temperature compensated and has a high coupling constant and high velocity. However, a disadvantage is the very accurate control requirement of the SiO film [12]. A promising material is 'Berlinite', certain cuts of which offer zero temperature coefficient of delay, high coupling constant and zero beam steering [15].

A comparison between several substrate materials in terms of their SAW parameters [12, 16] is given in Table 2-1.
Table 2-1

<table>
<thead>
<tr>
<th>Material</th>
<th>Orientation</th>
<th>Velocity m/sec</th>
<th>K² (%)</th>
<th>Temp. Coeff. of delay ppm/°C</th>
<th>Optimum Bandwidth (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LiNbO₃</td>
<td>Y-Z</td>
<td>3485</td>
<td>4.3</td>
<td>85</td>
<td>22</td>
</tr>
<tr>
<td>Quartz</td>
<td>Y-X</td>
<td>3159</td>
<td>0.22</td>
<td>-24</td>
<td>5.5</td>
</tr>
<tr>
<td>Quartz</td>
<td>ST-X</td>
<td>3158</td>
<td>0.17</td>
<td>0</td>
<td>4.5</td>
</tr>
<tr>
<td>Berlinite (AlPO₄)</td>
<td>X-Boule 80.4°</td>
<td>2751</td>
<td>0.7</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>SiO₂/LiTaO₃</td>
<td>Y-Z</td>
<td>3455</td>
<td>2.05</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>Bi₁₂GeO₂₀</td>
<td>(100)(011)</td>
<td>1681</td>
<td>1.4</td>
<td>-122</td>
<td>14</td>
</tr>
<tr>
<td>Tl₃VS₄</td>
<td>(110) Cylinder 24</td>
<td>1010</td>
<td>3</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>AlN/Al₂O₃</td>
<td>X-Z</td>
<td>6120</td>
<td>0.63</td>
<td>4.4</td>
<td>10</td>
</tr>
</tbody>
</table>

A Comparison in terms of SAW Parameters between Selected Common and New Piezoelectric Materials (Ref. [12] and [16])
2.3 THE INTERDIGITAL TRANSDUCER (IDT)

The IDT structure is shown in Fig. 2-1a. It consists of a series of interleaved electrodes made from a metal film deposited on a piezoelectric substrate. This structure, when driven by an electric signal induces an electric field in the substrate. This electric field sets up a surface wave through the piezoelectric effect. At a certain frequency, the launched waves from all the electrodes add in phase, in a constructive manner, and a condition of synchronism exists with the wavelength $\lambda$ of the launched acoustic wave equal to the period $L$ of the IDT. The synchronous frequency is $f_0 = v/\lambda$, where $v$ is the acoustic velocity. At this synchronous frequency, the transduction from electrical to acoustic energy is a maximum. By symmetry, surface waves are launched in two directions, so half of the acoustic energy is propagating in the required direction and the other half is absorbed by an acoustic absorber at the end of the crystal as shown. The propagating wave is in the form of alternating mechanical displacements with amplitudes decaying to negligible values in a depth of about a wavelength below the substrate surface $[17]$. A second transducer is used to detect the surface waves and converts them to an electric signal by the converse piezoelectric effect. This receiving transducer is also bi-directional and half of the incident acoustic energy passes under the transducer and is absorbed by an acoustic absorber at the other end of the crystal.

The IDT has been treated by Smith et al $[18]$ as an array of sources and the electrical properties of the transducer obtained directly. A single transducer can be represented by an equivalent circuit consisting of a capacitor $C_T$ in series with a resistor $R_a$. 
and an inductance $X_a$ (Fig. 2-1b). $C_T$ is the transducer capacitance, $R_a$ is the acoustic radiation resistance representing the amount of power transferred into acoustic energy and $X_a$ is the acoustic radiation reactance. Both $R_a$ and $X_a$ are frequency dependent. The transducer output is proportional to $N \frac{\sin[\pi(N+1)(f-f_0)]}{N\pi(f-f_0)}$ which illustrates the frequency selectivity of an $N$ period transducer.

There are four main parameters which can be used in transducer design [17]:

i) Periodicity of the fingers, controlling the centre frequency $f_0$.

ii) The number of finger pairs $N$, controlling the bandwidth.

iii) The overlap of the fingers, used to control the pass-band shape of the device.

iv) The aperture (finger length, $w$), used to control the impedance of the transducer for proper matching with electrical circuits.
FIGURE 2-1 a. Schematic representation of the generation, propagation and detection of surface acoustic waves

b. Series equivalent circuit for an interdigital transducer.
2.4 SAW DELAY LINES

The two IDT arrangements on a piezoelectric substrate shown in Fig. 2-1 form the non-dispersive SAW delay line, which is the basic SAW device. Many factors are of particular importance in delay line operation such as insertion loss, bandwidth and triple-transit signals [19]. In general, the requirements are for a SAW delay line with low insertion loss, broad bandwidth and high triple-transit suppression.

Bandwidth is material related and is controlled by the number of finger pairs in the transducer.

Insertion loss is due to many factors such as [20]: bi-directionality property of the IDT (3 dB loss in each transducer in matched condition), propagation attenuation, beam spreading, apodization, electrical mismatch and losses in the matching networks.

Triple-transit signals result when part of the acoustic power incident on the output transducer is reradiated as regenerated acoustic waves which propagate towards the input transducer, where they are again reflected and appear at the output as a spurious signal. Theoretically their level is 12 dB below the desired signal for perfectly matched delay lines. However, in unmatched delay lines the level is much smaller than this. A solution has been found for both insertion loss and triple-transit signals with the advent of the unidirectional transducer. This technique involves either a normal bi-directional IDT placed within a U-shaped multi-strip coupler, but offset from the centre by a $\frac{\lambda}{2}$ [21], or a multi-phase transducer [22] (Fig. 2-2) to achieve the necessary directionality which permits complete conversion from electrical to
acoustic signals travelling in one direction. This approach gives no bi-directional losses and very high triple-transit suppression as the output transducer can absorb all the incident acoustic power. The limitation to the U-shape m.s.c. and IDT technique is the requirement for high coupling coefficient materials, while in the multi-phase IDT approach is the complexity of the multi-layered electrode geometry. For many device applications high triple-transit suppression is achieved by mismatching the device [19].

Beside the triple-transit signals, in SAW delay lines there exists many other spurious effects. The most serious of these are: beam spreading with related diffraction effects and bulk wave generation. The design of SAW devices with high performance requires a good knowledge of SAW physics and SAW material properties.
Launched Wave

(a)

Multi-phase Electrical Input

(b)

FIGURE 2-2 a. Unidirectional transducer employing conventional IDT configuration and U-shape multi-strip coupler. (Ref 21)

b. Unidirectional transducer realized with multi-layered structure and multi-phase electric input. (Ref 22)
2.5 SAW FILTERS

The basic SAW device, the SAW delay line discussed in Section 2.4, in its simplest form is a band-pass filter. The output from the device is the convolution of the input with the impulse response of the device and is delayed in time with respect to the input. A uniform IDT, with N finger pairs, will convert an electrical impulse $\delta(t)$ applied across the electrical input terminals into rectangular surface wave pulse of N cycles. The fourier transform of such a pulse is of the form $\sin(f - f_0)/(f - f_0)$, which is the pass-band response of the transducer (Fig. 2-3). The impulse response of the transducer is directly related to its geometry. With amplitude and phase weighting on the IDT any desired impulse response (which is the inverse Fourier transform of the required frequency response) can be obtained.

In general, the frequency response of the delay line is the product of the responses of its two transducers [19]. Controlled shape factors and side-lobe levels band-pass filters can be realized with SAW delay lines, in which the first transducer is apodized (weighted) in accordance with the desired impulse response and the second transducer is a broad-band with only few finger pairs (Fig. 2-4 explains this principle). Other arrangements using multi-strip couplers (MSC) are also possible [20], but are limited to high $K^2$ materials.

Referring to Fig. 2-4, as the second transducer is a wide-band one, so the filter characteristics depend mainly on the apodized IDT. However, the wide-band transducer will cause undesired rounding of the filter response due to its own $\sin x/x$ property. Because the length of the substrate is finite, a truncating of the
impulse response is necessary. This, in the frequency domain,
gives rise to in-band ripple, sidelobes and less steepness \[23\].
Optimum design will result in minimum impulse response length \(T\)
while meeting the specifications. Important performance parameters
are \[24\]: centre frequency, bandwidth, steepness, sidelobe level
and bandpass ripples. These parameters are also schematically
defined in Fig. 2-4.

SAW bandpass filters have been of great interest in recent
years and a lot of work has been done in this area. This arises
from the fact that SAW filters offer many advantages over conven-
tional filters, these are \[5\]:

i) small size - compatible with IC technology.

ii) ruggedness.

iii) stability - no requirements for adjustment after manufacturing.

iv) reproducibility

v) flexibility - filter characteristics can be easily controlled
   by weighting technique.

vi) light weight.

vii) high frequency operation.

SAW filters have been found to be particularly suitable for
high VHF and UHF requirements \[24\]. Narrow bandpass filtering in
the UHF region can now be easily realized with SAW resonators, which
are new SAW devices characterised by their frequency selective
reflecting array and capability to operate with very high \(Q\) at such
high frequencies. Other filtering functions such as discrete and
continuous bandpass filters, fixed and programmable matched filters
are possible with SAW technology.

One device which has found successful application in radar
as it permits high signal to noise ratio and high resolution with reduced transmitting pulse energy, is the dispersive filter. Such a filter is shown in Fig. 2-5. Here a dispersive relation, \( \Delta f \) over a period \( T \), is achieved by graded periodicity in the transducer. When the transmitting dispersive transducer is excited with a voltage pulse a chirp signal, which is the impulse-response of the device, is generated having a time length \( T \), and a linear frequency sweep \( \Delta f \). In the receiver a similar filter with opposite dispersion is required, as shown, to detect the echo pulse. Its output is the fourier transformation of the input pulse envelope with length equal to \( 1/\Delta f \) and delayed by \( t_d[25] \), the delay line length. This reconstitution of a short pulse from a long transmitted pulse is known as 'pulse compression'. With the uniform configuration shown in Fig. 2-5 the output from the receiving pulse compression filter, PCF, produces high time sidelobes. However these can be minimised by applying a weighting function to the amplitude response of the pulse compressor [26]. This indicates how with SAW technology it is possible to combine two signal processing functions in a single device. In a similar way it is possible to generate, detect and compress, not only signals with linear frequency dispersive relation \( \Delta f \) but other coded signals as well [27].

SAW devices with reflective arrays form the base for many useful devices. These reflective arrays, formed from a set of metal strips or grooves, can be used to change the passband response, lengthen the delay time or improve the device performance [8]. Three examples of SAW devices incorporating reflective arrays are presented in Fig. 2-6. Device 'a', a reflective array compressor (RAC), consists of two sets of angled grooves, each with graded
periodicity. Incident surface waves launched from the input IDT are reflected twice through 90° towards the output transducer. This type of pulse compression filter (PCF) gives lower second order effects as compared with IDT types (Fig. 2-5) and time bandwidth (TB) products up to $10^4$ [28]. Device 'b' uses a similar principle to achieve a bandpass filtering function [29]. Here one array, with uniform periodicity, is used and the input and output IDTs are at right angles. Weighting can be achieved by varying the length of the grooves. An extension to this device is the use of several arrays, of different centre frequencies, in the path of one SAW beam with one IDT for each array so that the device operates as a bank of bandpass filters.

Narrow bandpass filters operating at UHF such as the SAW resonators - detailed in Chapter 3, have also been realised with reflective arrays (device 'c' in Fig. 2-6). Here two arrays are normally used to form a SAW resonant cavity. Each array consists of large numbers of grooves or deposited metal strips providing reflection coefficient very close to unity when the incident surface wave has a wavelength $\lambda$ equal to two times the array's period. Coupling can be achieved by single or double IDTs placed in the cavity.
FIGURE 2-3. Uniform IDT response, in time and frequency domain to an electrical impulse $\delta(t)$. 

$\text{Impulse Response} \quad \text{Frequency Response}$

$\text{rect}(t/T) \cos \omega t \quad \frac{\sin[(\omega_0-\omega)T/2]}{(\omega_0-\omega)T/2}$

FIGURE 2-4. Controlled shape factors and sidelobe level can be obtained with proper IDT weighting.
FIGURE 2-5. SAW Dispersive filter principle
(a) Transmitting linear FM pulse generator
(b) Receiving pulse compression filter
FIGURE 2-6. Reflective arrays are the base for many SAW devices.
2.6 SAW DEVICES AND APPLICATIONS

SAW delay lines of composite structures or with external electronic circuiting offer, beside the filtering functions discussed in the previous section, a range of very useful devices such as oscillators, variable delay lines, Fourier transform processors, convolvers and correlators [8], etc.

SAW devices show exciting potential in many areas of application due to the following important features [5, 28]:

i) Wide fundamental frequency range of operations covering VHF, UHF and lower micro-wave frequencies.

ii) IDT Configuration offers spatial display and control sampling in real time.

iii) Passive signal processing at high dynamic range.

iv) Planar, simple, comparable with micro-electronic IC manufacturing techniques.

Table 2-2, extracted from ref. 5, summarises most of the primary areas of application of SAW devices and their derivatives. The detailed discussion of this table is beyond the scope of this thesis, but most of the devices and their applications are reported in references [4, 30, 31]. In radar, consumer and military electronics SAW devices have found established applications [32]. Current areas of SAW application assessments are very large and have been subject to extensive study.

One class of SAW device, the oscillators (both delay line and resonator stabilised), is potentially useful for applications in radar and communications, where they can be used as rugged stable frequency sources operating at high fundamental frequencies (see Chapter 3). Also delay stabilised SAWOs, when designed with
voltage control capability, are attractive for use in the digital frequency synthesisers required for agile radar, navigation and multi-channel communications systems. SAW oscillator applicability to single and multi-channel indirect synthesisers has been the primary concern of the research described in this thesis.
<table>
<thead>
<tr>
<th>Device</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay Line</td>
<td>Fusing, MTI Radar, Communications Path Length Equaliser, Altimetry, Time Ordering</td>
</tr>
<tr>
<td>Wideband Delay Line</td>
<td>Recirculating Digital Storage</td>
</tr>
<tr>
<td>Bandpass Filter and Resonator</td>
<td>Colour TV, Radar, Communications Satellite Repeaters, ECM, Frequency Synthesis</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Stable Source VHF to Microwave - Communications and Radar</td>
</tr>
<tr>
<td>Tapped Delay Line</td>
<td>Fourier Transformation, Acoustic Image Scanning, Clutter-Reference Radar, SSR, ECM Deception</td>
</tr>
<tr>
<td>MATCHED FILTER Dispersive Delay Line ('CHIRP')</td>
<td>Radar Pulse Compression, Variable Delay for Target Simulation, Fourier Transformation (Spectral Analysis), Compressive Receiver, Group Delay Equalisation</td>
</tr>
<tr>
<td>FSK Filter</td>
<td>Spread Spectrum Communications, Radar, Military ATC</td>
</tr>
<tr>
<td>Convolver</td>
<td>Synchroniser for Spread Spectrum Communications, Fourier Transformation</td>
</tr>
</tbody>
</table>

Table 2-2
Prime Applications of SAW Devices (Ref. [5])
CHAPTER III

FREQUENCY SOURCES

3.1 INTRODUCTION

Current VHF/UHF communications are commonly based on two types of frequency sources, LC- and crystal-controlled oscillators. LC oscillators are capable of operating directly in the VHF/UHF region, but they are unstable and difficult to design for a precise frequency [33]. However, their tuning range (bandwidth) is large enough to cover the whole band required for multi-channel Transmit/Receive radio telephone applications. On the other hand, crystal-controlled oscillators are highly stable but the upper limit of their fundamental frequency is \( \sim 30 \) MHz and their tuning range is poor (\( \sim 0.05\% \)).

Recently a new class of frequency sources, SAW oscillators, [34, 35] has appeared, possessing features which make them very attractive for many areas of application. These features are:

i) fundamental mode of operation at frequencies from \( \sim 20 \) MHz up to 2GHz.

ii) ruggedness in construction.

iii) immunity to shock and vibration [36].

iv) good phase-noise performance [37, 38].

v) very high oscillator Q's can be obtained.

vi) moderate tuning range.

vii) high output power capability (\( \sim 1w \)).

Table 3-1 gives a comparison of properties of various oscillators.

In this chapter, LC and crystal oscillators are first
discussed. Then SAW oscillators, both delay line and resonator stabilized, are covered in detail. This is followed by a section on frequency stability with particular emphasis on oscillator 'phase-noise' performance due to its importance for system applications.
<table>
<thead>
<tr>
<th>Oscillator type</th>
<th>Operating mode</th>
<th>Frequency range (Hz)</th>
<th>Effective loaded Q</th>
<th>Deviation</th>
<th>Temperature coefficient (-30 to + 70°C) (parts in 10^6/deg C)</th>
<th>S.s.b. f.m. noise at 10k Hz offset from 500 MHz source dB/Hz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional quartz crystal</td>
<td>resonator stabilized</td>
<td>10^4-3x10^7 (fundamental)</td>
<td>5x10^3-2x10^6</td>
<td>up to 500 parts in 10^6</td>
<td>&lt;1</td>
<td>-140 (multiplied 10 MHz)</td>
</tr>
<tr>
<td>LC-based voltage controlled</td>
<td>resonator stabilized</td>
<td>10^3-10^10</td>
<td>10^1-10^3</td>
<td>up to octave bandwidth</td>
<td>typically 10</td>
<td>-100</td>
</tr>
<tr>
<td>Surface acoustic wave</td>
<td>resonator stabilized</td>
<td>10^7-2x10^9</td>
<td>10^4-10^5</td>
<td>&lt;100 parts in 10^6</td>
<td>approximately -140</td>
<td>-105 to -140 (Q dependent)</td>
</tr>
<tr>
<td></td>
<td>delay stabilized</td>
<td>10^2-10^4</td>
<td>10^8-10^2 parts in 10^6</td>
<td>-1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3.2 GENERAL FORM OF OSCILLATOR CIRCUIT

The general form of an oscillator is shown in Fig. 3-1. It consists of an amplifier with gain 'A' and a feedback network 'β'. To sustain oscillation two conditions must be satisfied [39]:

i) The total phase shift introduced, as a signal proceeds from the input terminals, through the amplifier and feedback network, and back again to the input, is precisely zero (or, an integral multiple of 2π). In other words

\[ \theta \text{ around the loop } = n(2\pi) \]

where \( n \) is an integer.

ii) The magnitude of the total gain around the loop must not be less than unity, or

\[ A\beta = 1 \quad (3.1) \]

where \( A \) = amplifier gain

\( \beta \) = feedback factor.

The unity loop gain condition requires a single and precise value for amplifier gain. In practice, amplifiers gains are changeable due to circuit component and transistor change characteristics with age, temperature, voltage, etc. If the loop gain becomes less than unity the oscillation stops. If it becomes larger than unity the oscillation will build up until circuit non-linear elements limit its amplitude. So in practical oscillators the loop gain is designed to be slightly larger than unity, and the amplitude of oscillation is limited by the onset of circuit non-linearity.
Oscillating conditions:

\[ A \beta = 1 \]

Phase shift \((\theta)\) round the loop = \(n(2\pi)\)

Fig. 3-1 General form of oscillator loop
3.3 LC AND CRYSTAL OSCILLATORS

Basically, LC and crystal oscillators are resonant oscillators in which the feedback 'β' is accomplished through a resonant circuit. A general circuit configuration valid for both LC and crystal oscillators is shown in Fig. 3-2. The voltage across $Z_1$ is fed back in series with the amplifier input. The type of circuit elements employed for the resonant network determines the form of oscillator as described below:

(1) **LC Oscillators:**

In LC oscillators, the impedances $Z_1$, $Z_2$, and $Z_3$ in Fig. 3-2 consist of reactances $X_1$, $X_2$, and $X_3$ and the phase condition for oscillation requires [39]:

$$X_1 + X_2 + X_3 = 0 \quad (3.2)$$

Also the loop gain is given by:

$$\beta = \frac{-A_v X_1}{X_1 + X_3} \quad (3.3)$$

Or, using Eq. (3.2)

$$\beta = \frac{+A_v X_1}{X_2} \quad (3.4)$$

As $\beta$ must be positive and $A_v$ is also positive, $X_1$ and $X_2$ must have the same sign, i.e., they must be the same kind of reactance and opposite to $X_3$ [$(X_3 = -(X_1 + X_2)$, Eq. (3.2)]. If $X_1$ and $X_2$ are capacitives, $X_3$ must be an inductance, hence a Colpitts oscillator is realized. If $X_1$ and $X_2$ are inductances, $X_3$ must be a capacitance, and a Hartely oscillator is obtained.

LC oscillators form the current sources in the VHF/UHF frequency band for synthesiser application. However, their frequency
stability and quality factor 'Q' are both poor. Q values at VHF typically vary between 100 and 500. However, well designed oscillators can exhibit higher Q \[140\]. Varactor diodes are commercially available with electronically tunable capacitance ratios between 2:1 and 10:1. These allow the design of VHF and UHF electronically tunable LC voltage controlled oscillators (LC-VCO) with octave bandwidths.

(2) Crystal Oscillators:
In crystal oscillators, the frequency determining circuit is obtained using a piezoelectric crystal, usually Quartz. Such a crystal, properly orientated and placed between two electrodes will vibrate when excited with electrical signal. The amount of crystal vibration depends on the frequency of the applied voltage. At certain frequency, \( f_0 = \frac{K}{t} \) where \( K \) is a constant that depends on the crystal cut and other factors and \( t \) is the crystal thickness, the crystal vibrations reach a maximum. Due to the piezoelectricity property, this vibration has associated with it an electric potential. The resonant frequency and the Q depend upon the crystal dimensions, orientation and mounting \[141\]. Crystals with fundamental frequencies of between 10 KHz and 30 MHz and Q factors from \( 10^3 \) to \( 1 \times 10^6 \) are obtainable \[142\] but the most stable types are those using AT cut quartz whose fundamental frequencies range from 2 to 20 MHz. The long term frequency stabilities of such crystals can be small fractions of 1 ppm per month. Frequencies between 30 and 100 MHz can be obtained either by special crystal manufacturing techniques \[143\] or by using overtone crystals, but these are less efficient and their stability is poorer.
The electrical equivalent circuit of the crystal together with its reactance characteristics are shown in Fig. 3-3. $L_1$, $R_1$ and $C_1$ account for the crystal mechanical resonance parameters while $C_2$, the mounting capacitance, represents the electrostatic capacitance between electrodes with the crystal as a dielectric and is very much larger than $C_1$.

As shown in Fig. 3-3c the crystal has two resonant frequencies, a series resonance $f_s$, $f_s = 1/(2\pi \sqrt{L_1 C_1})$, and a parallel resonance $f_p$, $f_p = 1/(2\pi \sqrt{C_p})$ where $C_p = \frac{\frac{C_1 C_2}{C_1 + C_2}}{C_1 + C_2}$. However, due to the fact that $C_2 \gg C_1$, these frequencies are nearly equal. Also for frequencies $f_s < f < f_p$ the crystal reactance is inductive and for all other frequencies it is capacitive.

The crystal's Q is defined as the ratio of the equivalent inductive reactance to resistance, $Q = \frac{2\pi f_s}{L_1/R_1}$ [44], where $f_s$ is the series resonant frequency. Many configurations of crystal controlled oscillator are possible. One approach is to replace $Z_1$ in the basic circuit of Fig. 3-2 by a crystal, $Z_2$ by LC combination and $Z_3$ by the drain to gate capacitor of an FET transistor connected as shown in Fig. 3-3d [39]. To meet the oscillation condition stated in Eq. (3.2), the crystal and LC network reactances must be inductive. The circuit oscillates at a frequency, determined essentially by the crystal, which lies between $f_s$ and $f_p$ (see Fig. 3-3c).
Fig. 3-2 The basic configuration for many resonant circuit oscillators (Ref. 39).
FIGURE 3-3. The crystal resonator:
(a) Crystal symbol.
(b) Electrical equivalent circuit of the crystal.
(c) The crystal reactance function (for $R_t=0$).
(d) Crystal stabilized oscillator circuit.
3.4 SAW DELAY LINE STABILIZED OSCILLATOR

3.4.1 Basic Theory

The basic arrangement of the delay line stabilized oscillator is shown schematically in Fig. 3-4. It consists of a SAW delay line with an amplifier connected to form a positive feedback, i.e. regenerative circuit in which the SAW delay line forms the feedback network. With greater than unity loop gain oscillation occurs when the phase transfer round the loop is an integral multiple of \( 2\pi \) (i.e. the frequency of oscillation must satisfy the condition that there is an integral number of wavelengths round the loop). Each discrete frequency which satisfies this condition corresponds to a possible mode of oscillation. The mathematical equations governing the oscillator operation can be derived as follows [45]:

If \( \phi_N \) is the phase shift experienced by a signal as it proceeds completely round the loop and \( N \) is a number of wavelengths (\( N \) is an integer by the loop phase condition), then we have:

\[
\phi_N = 2\pi N
\]  
(3.5)

Defining the effective length of a delay line using uniform interdigital transducers as the distance between the midpoints of those transducers, we have: \( L_{d,L} \equiv \text{effective length}, \tau \equiv \text{delay time}, \phi_{d,L} \equiv \text{phase shift}, N_{d,L} \equiv \text{number of wavelengths in the delay line}.

Thus:

\[
\phi_{d,L} = 2\pi N_{d,L}
\]  
(3.6)

\[
L_d = N_{d,L} \lambda
\]  
(3.7)

and \( v_s = \frac{L_{d,L}}{\tau} \)  
(3.8)

where \( \lambda = \text{the wavelength} \)
and \( v_s \) = the velocity of the surface wave.

Now, \( v_s = f \lambda \) \hspace{1cm} (3.9)

The frequency \( (f) \) of oscillation with \( N \) wavelengths round the loop is therefore given by:

\[
f = \frac{v_s}{\lambda} = v_s \frac{N d_L}{L d_L} = \frac{v_s N}{L d_L}
\] \hspace{1cm} (3.10)

Since \( N = \frac{N d_L}{d L} \), as the great majority of wavelengths round the loop are in the delay line.

Using Equations (3.6) and (3.10), then:

\[
\phi_{d_L} = \frac{2\pi L d_L f_N}{v_s}
\] \hspace{1cm} (3.11)

where \( f_N \) is the frequency of oscillation with \( N \) wavelengths round the loop. The phase condition for oscillation, Eq. (3.5), may thus be written as

\[
\frac{\omega N d_L}{v_s} + \phi_E = 2\pi N \] \hspace{1cm} (3.12)

\( \phi_E \) is the phase shift through the transducers and the maintaining amplifier.

From Eq. (3.10) it is evident that the loop is capable of oscillating at a comb of frequencies where the frequency separation between modes with \( N \) wavelengths and \( (N - 1) \) wavelengths round the loop, using Eq. (3.8), is given by

\[
\Delta f = f_N - f_{N-1} = \frac{v_s}{L d_L} = \frac{1}{\tau} \] \hspace{1cm} (3.13)
3.4.2 The Quality Factor

The quality factor 'Q' yields a measure of oscillator stability. In resonator stabilized oscillator circuits, Q is defined in terms of the ratio of energy stored to energy lost or alternatively in terms of the passband characteristics as shown below [45, 46].

The phase of a parallel resonant circuit is given by:

\[ \phi = \tan^{-1}\left(\frac{\frac{1}{\omega_c} - \omega L}{R}\right) \]  \hspace{1cm} (3.14)

where \( R \) = resistance; \( c \) = capacitance, \( L \) = inductance and \( \omega \) = angular frequency.

At \( \omega = \omega_0 \) (where \( \omega_0 = \frac{1}{\sqrt{LC}} \) resonance condition), the phase slope is derived from Eq. (3.14) by differentiation.

\[ \frac{d\phi}{d\omega} = \frac{2}{\omega_0} \cdot \frac{\omega L}{R} \]  \hspace{1cm} (3.15)

Since the Q of a parallel resonant circuit can be defined by:

\[ Q = \frac{\omega_0 L}{R} \]  \hspace{1cm} (3.16)

Then, Eq. (3.15) can be written again as

\[ \frac{d\phi}{d\omega} = \frac{2}{\omega_0} \cdot Q \]  \hspace{1cm} (3.17)

From Eq. (3.17) Q can be defined in terms of the phase slope as

\[ Q = \frac{\omega_0}{2} \cdot \frac{d\phi}{d\omega} \]  \hspace{1cm} (3.18)

A SAW delay line is a non-resonant frequency stabilizing element and thus has no Q value defined in the conventional way. However, Eq. (3.18) shows that for conventional oscillators
the phase slope $\frac{d\phi}{d\omega}$ is the factor which determines the $Q$ value. Thus for the SAW delay stabilized oscillator an approach using the phase slope of the SAW delay line response can lead to a definition for their $Q$.

The phase slope of a non-dispersive delay line of delay is given by:

$$\frac{d\phi}{d\omega} = \tau$$

(3.19)

Comparing equations (3.18) and (3.19), it can be seen that the $Q$ of a delay line based on its phase slope is given by:

$$Q = \frac{\tau \omega}{2} = \tau \pi f_0$$

(3.20)

Since, $\tau = \frac{\lambda}{v_s}$ and $\lambda = N\lambda$, then equation (3.20) becomes

$$Q = \frac{N\lambda \pi f_o}{v_s}$$

(3.21)

But $\lambda/v_s = 1/f_0$, so the $Q$ of SAW delay stabilized oscillator is defined by

$$Q = \pi N$$

(3.22)

### 3.4.3 Mode Selection

Equations (3.10) and (3.13) show that the oscillator loop can support a comb of frequencies $f_N = \frac{v_sN}{L_dL}$ separated by $\Delta f = \frac{1}{\tau}$. Here the separation between the possible oscillation modes is inversely proportional to $N$, which is the number of wavelengths round the loop. However, the frequency selectivity of an IDT can be used to achieve mode-selection [35/45]. The $\sin x/x$ response of the IDT, Fig. 3-5, depends on the number of finger
pairs (P) in the main transducer. The peak of the response occurs at the fundamental frequency of the IDT $f_0$ and the nulls of the response occur at

$$f = f_0 \pm \frac{f_0}{P}$$

(3.23)

If the value of $P$ is smaller than $N$, then the oscillator is subject to multi-moding (this forms a class of SAWO operation of interest for certain applications) \[47\]. In this type of operation the phase angle required for oscillation occurs several times within the passband of the IDT as demonstrated in Fig. 3-5. If the value of $P$ is chosen equal to $N$, then nulls of the response occur at

$$f = f_0 \pm \frac{f_0}{N}$$

(3.24)

Having in mind that the separation between the modes is $f_0/N$ [Eq. (3.13)], then it is clear that oscillation now occurs only at the frequency $f_0$ of the response peak and the other modes are suppressed as they are located at the amplitude nulls of the response at which points the loop gain is zero. With this arrangement the amplitude nulls are rotated $360^\circ$ from the phase angle at $f_0$. Fig. 3-6 shows how the $\sin x/x$ response of the main transducer is used for mode selection. In practice, the IDT with an open structure geometry (tapped transducer) is usually used for mode selection \[35\]. Here the combined frequency response of two transducers, separated by an effective length equal to the total length of both transducers is used to suppress all unwanted modes as shown in Fig. 3-7 \[48\]. Here the tapped transducer gives a series of main peaks at frequencies $f_n = n/R$. The distance between each peak first nulls is $\pm 1/MR$. Mode selection is achieved first by making
the length of the short transducer equal to \( R \) (the separation between taps), so the main peak at frequency \( f_0 \) is selected and second, by making the delay line length \( L \) equal to \( MR (= P + R) \) so that one mode is selected within this selected peak. This approach has the advantage of better stability, as it allows an increase in the effective length of the delay line and reduced distortion in the frequency response, as it permits the use of a small number of finger pairs in the large transducer, resulting in less metalization.

3.4.4 Frequency Modulation

Referring to Eq. (3.18), an expression for a fractional frequency change can be found in terms of the quality factor \( Q \) which takes the form \([45]\)

\[
\frac{\Delta \omega}{\omega} = \frac{\Delta \phi}{2Q}
\]  

(3.25)

But \( Q = \pi N \) \([\text{Eq. (3.22)}]\), then

\[
\frac{\Delta \omega}{\omega} = \frac{\Delta \phi}{2\pi N}
\]  

(3.26)

Which means that any small phase change introduced in the loop will be accompanied by the fractional frequency change given by Eq. (3.26).

The most suitable way to introduce a phase change is through the loop circuit elements outside the delay line by the use of a phase shifting network as shown in Fig. 3-8. A phase shift of \( \pm \frac{\pi}{2} \) caused by this network will introduce a fractional frequency change of \( \pm 1/4N \) which can be obtained from Eq. (3.26) by substituting \( \Delta \phi = \pm \frac{\pi}{2} \).
\[ \frac{\Delta \omega}{\omega} = \frac{\Delta \phi}{2\pi N} = \pm \frac{\pi/2}{2\pi N} = \pm \frac{1}{4N} \tag{3.27} \]

Note that \( \pm \frac{\pi}{2} \) is a small quantity compared to the number of wavelengths \( N \) in the delay line. It is not practical to exceed \( \pm \frac{\pi}{2} \) phase shift as this will lead to the operating point becoming too far removed from the delay line response peak. This will produce increased delay line insertion loss, which may result in failure of oscillation if the amplifier can no more maintain the required loop gain.

As can be seen from Eq. (3.27), the frequency modulation capability of delay stabilized SAWO's is inversely proportional to the length of the delay line \( (N) \), hence to the oscillator \( Q \) [Eq. (3.22)]. It is possible therefore, during design to trade off the oscillator \( Q \) to give either high stability \( (Q \sim 1 \times 10^4) \) or a frequency deviation capability up to 1% of the operating frequency \( (Q \sim 100) \).
FIGURE 3-4. Basic SAW delay-line oscillator

FIGURE 3-5. Frequency modes for SAW oscillator with a delay line in which the number of finger pairs 'P' is smaller than the IDT separation 'N'.
FIGURE 3-6. Mode selection in SAW oscillator employing a delay line in which the number of finger pairs 'P' is equal to the time delay 'N'.

H'I
P=N
N
Frequencies for \( \omega T+\theta = 2n\pi \)

\begin{align*}
fo &- \frac{2fo}{N} \\
fo &- \frac{fo}{N} \\
fo & \\
fo &+ \frac{fo}{N} \\
fo &+ \frac{2fo}{N}
\end{align*}
A SAW delay line with open structure IDT.

(b) Frequency response of long transducer.

(c) Frequency response of short transducer.

(d) Response of the delay line $\propto b \times c$.

FIGURE 3-7. SAW delay line oscillator mode selection with tapped transducer. Mode selection is achieved by making the short transducer length $R$ equal to the separation between taps and the length of the delay line $L$ equal to $P + R = MR$. 

$$f_o \left(1 - \frac{1}{P+R}\right)$$

$$f_o \left(1 + \frac{1}{P+R}\right)$$

$$f_o$$
FIGURE 3-8. SAW delay line controlled oscillator with frequency modulation capability.
3.5 SAW - RESONATOR STABILIZED OSCILLATORS

3.5.1 The SAW Resonator

The surface acoustic wave resonator is a relatively new device which has recently received considerable attention. This device has been found to be broadly equivalent to the bulk crystal resonator presently in use for oscillators and filters. However, SAW resonators have the following advantages when compared to bulk resonators:

i) fundamental frequency of operation with high Q extends through the VHF/UHF frequency range compared to ~30MHz practical upper limit for fundamental operation of bulk wave resonators.

ii) Q is insensitive to crystal thickness.

iii) They are rugged and small in size.

iv) SAW resonators offer a greater tuning and trimming capability.

A SAW resonator consists of two reflectors, each of which consist of a large number of 'reflection sections' (perturbations) on the surface of a piezoelectric crystal periodically spaced one half wave length (\(\lambda/2\)) from centre to centre. Every reflection section consists of a \(\lambda/4\) wavelength 'reflecting element' of impedance \(Z_1\) and a \(\lambda/4\) wavelength 'gap' of impedance \(Z_0\). Each reflection section forms an impedance discontinuity of \(Z_1/Z_0\). Typically, 0.1 - 0.3 per cent of the incident surface wave energy is reflected from a single reflecting element \([49]\), therefore several hundred elements are required in each reflector to achieve proper operation. Two reflectors form a SAW cavity. Many resonator configurations are possible \([50]\), however, the most common consists of a pair of
reflectors with one or two coupling transducers placed within the cavity to form a one-part or two-part resonator respectively. A two-part resonator device is shown schematically in Fig. 3-9.

For a resonator device, important design parameters are [49]:

i) Maximum input and output coupling to the acoustic energy in the cavity.

ii) The physical cavity size (the distance between the inside edges of the reflectors).

iii) The positioning of the coupling transducers inside the cavity.

iv) The reflection coefficient of the reflectors.

v) Suppression of unwanted modes.

3.5.2 The Surface Wave Cavity

A surface wave cavity may be formed by using two reflectors which reflect the surface wave back and forward many times. Each reflector consists of several reflection sections, each of which has a very small contribution to the reflection process. The incident acoustic energy will penetrate some distance into the reflector structure, Fig. 3-10. This distance depends on the type of the reflecting elements and the substrate in use and is given by [49]:

\[ x = \frac{\lambda}{4\Delta Z} \]  \hspace{1cm} (3.28)

where \( \lambda \) = the wavelength

\( \Delta Z \) = a quantity depending on the impedance discontinuity of the reflection section and given by \( \Delta Z = \frac{Z_1}{Z_0} \) [51].

The incident surface wave, when penetrating the reflectors,
undergoes small reflections at each reflection section. These reflections add in phase over a narrow frequency band when the array period is equal to a half wavelength \([51]\). Outside this frequency band, most of the energy incident on the reflectors is transmitted. Typical fractional bandwidths of SAW resonators are 0.1% or less.

The added reflections from successive reflection sections in the reflecting array gives a total reflection coefficient \(\Gamma\) given by \([52]\):

\[
|\Gamma| = \frac{|Z_1 - Z_0|}{|Z_1 + Z_0|}^{2M} - 1 \tag{3.29}
\]

where, \(M\) = number of equal width strips (reflecting elements) and gaps. The value of \(|\Gamma|\) must be near unity (\(> 0.98\)) for proper operation.

For the surface wave cavity an important factor is the spacing (in wavelengths \(\lambda\)) between the inside edges of the reflectors. If this spacing is an integral number of half-wavelengths, then the cavity will resonate and an acoustic standing wave will exist between the reflectors. But if this spacing is an integral number of half-wavelengths plus a quarter wavelength \((\lambda/4)\), then the cavity will be anti-resonant as no reinforcing for the surface wave will take place. The spacing also must be selected so as to limit the number of modes, as multi-moded operation may take place within the bandwidth of the reflectors when the cavity length becomes large \([53]\). The effective cavity length is given by \([50]\):

\[
L = D + 2X \tag{3.30}
\]

where
D = separation between reflectors
X defined in Eq. (3.28).

The SAW cavity is coupled to an electrical circuit through an IDT as shown in Fig. 3-9. The IDT must be placed symmetrically between the reflectors and such that its excitation field pattern couples to the standing wave field pattern of the cavity. Maximum coupling occurs when the IDT electrodes are positioned on the peaks of the standing wave set up at resonance. Any deviation from this position will reduce the coupling. The standing wave peaks, and hence the IDT electrodes positions, can be determined during design when deciding the material to be used. At the present time, the most common materials used for resonators are ST-Quartz and LiNbO₃. For ST-Quartz the nulls of the standing wave occur at the edges of the first reflecting elements in the array while for Lithium-niobate the peaks of the standing wave occur at the edges of the first reflecting elements, Fig. 3-11[54].

The maximum IDT size is limited by the requirement that the transducers be in the cavity and that the cavity be small so that it will support only one resonance mode[53]. The design of the transducer also controls the impedance of the completed resonator.

3.5.3 A SAW Resonator Equivalent Circuit

Simple electrical equivalent circuits in which the circuit elements are related to the physical design parameters of one-port and two-port resonators have been developed[51/52]. These equivalent circuits lead to the prediction of the important parameters of the SAW resonators such as the quality factor 'Q', bandwidth and loss.
Fig. 3-12 shows the equivalent circuits for both one-port and two-port SAW resonators, which are valid near resonance. In both circuits, \( R_0 \) and \( C_0 \) are, respectively, the radiation resistance and static capacitance in the shunt model of the IDT alone and they are given by \[18/52\]:

\[
C_0 = N C_s W \quad (3.31)
\]

\[
R_0 = \left[ 8 K^2 f_o N^2 C_s W \right]^{-1} \quad (3.32)
\]

where \( N \) = the number of pairs of electrodes in the IDT

\( C_s \) = capacitive per one millimetre finger length

\( W \) = the aperture width of the IDT.

\( K^2 \) = the substrate electromechanical coupling constant.

\( f_o \) = the resonant frequency.

For reflection coefficient \( |\Gamma| = 1 \), the other circuit elements \( R_1, L_1 \) and \( C_1 \) are given by the following expressions with the condition that in the two-port resonator the IDTs are identical \[52\]:

\[
R_1 = \frac{1 - |\Gamma|}{2|\Gamma|} R_0 \quad (3.33)
\]

\[
L_1 = \frac{L}{4 f_o |\Gamma|} R_0 \quad (3.34)
\]

\[
C_1 = \frac{1}{(2\pi f_o)^2 L_1} \quad (3.35)
\]

where, \( |\Gamma| \) and \( L \) are defined in Equations (3.29) and (3.30) respectively.

The unloaded \( Q_u \) of the resonator is then given by:

\[
Q_u = \frac{\omega_0 L_1}{R_1} \quad (3.36)
\]
Referring to Fig. 3-12, it can be seen that the equivalent circuit of one-port resonator is similar to that of a bulk-crystal resonator. Near resonance the transducer couples strongly to the fields in the cavity and its impedance is loaded by the low-impedance of the series arm \((R_1, L_1, C_1)\). Because \(C_0\) is shunting the series arm, then two resonance cases are obtained. Series resonance \((f'_1)\) due to the series arm and parallel resonance \((f'_2)\) due to \(C_0\) with \(L_1C_1\). The resonance frequencies are very close to each other. At \(f'_1\) the reactance of the circuit is zero while at \(f'_2\) it is infinity. This type of operation has the disadvantages of limited bandwidth and less attenuation away from resonance [55]. These limitations are avoided by the two-port SAW resonator which has the advantage that the capacitance \(C_0\) does not parallel the resonant arm and a single resonance will occur.

In both one-port and two-port resonators, away from resonance the majority of the incident waves at the reflectors are transmitted, the impedance of the series arm \((R_1, L_1\) and \(C_1\)) becomes very large and the impedance of the system is determined by the IDT alone \((R_o, C_o)\).
**FIGURE 3-9.** The two port SAW resonator configuration

**FIGURE 3-10.** Distributed reflector operation

\[ x = \frac{\lambda}{4\Delta Z} \]
FIGURE 3-11. The SAW resonator standing wave nodes and anti-nodes positions for Al on LiNbO (a) and Al on ST Quartz.

FIGURE 3-12. SAW resonator equivalent circuit.

(a) One-port  (b) Two-port
3.6 FREQUENCY STABILITY

3.6.1 Definition

Frequency stability is defined as "the degree to which an oscillating signal produces the same value of frequency for any interval, $\Delta t$, through a specified period of time" [56] and is normally divided into three regions; long-term stability, medium-term stability and short-term stability. These are explained below.

1. Long-Term Stability:
This factor is usually expressed in terms of parts per million of frequency change per year. It represents a predictable frequency variation due to ageing processes of the material used in the frequency determining element and changes in circuit component values.

2. Medium-Term Stability:
This is defined as the shift in oscillator frequency due mainly to changes in temperature and is primarily determined by the temperature coefficient of phase shift through the frequency controlling element and the maintaining amplifier.

3. Short-Term Stability:
Short-term stability is a function of the frequency fluctuations about the nominal frequency in a period of a few seconds. Frequency fluctuations of this nature are related to the noise sidebands in the oscillator output [57] and short-term stability is frequently referred to as the 'phase-noise' performance of the oscillator under consideration.

Phase-noise is a factor which has important effects in real
systems. Today's equipment demands signal sources with improved phase-noise characteristics. Excessive phase-noise limits the performances of many systems in different ways. In doppler radars, for example, phase-noise on either the transmitter exciter or the receiver local oscillator can limit range, resolution and sensitivity. Another example is the effect of phase-noise on multi-channel communication receivers. Here the local oscillator phase-noise sidebands appear on the received signal in the IF channel at the same ratio as they exist on the local oscillator. The level of these sidebands at an offset equal to the channel spacing sets a limit on the sensitivity of the receiver.

The 'phase-noise' of any oscillator can be explained as follows: Referring to Fig. 3-13, the input stage of the amplifier is a major noise source. This results in noise sidebands in the oscillator output, the spectral density of which show a continuous spectrum over a wide range of frequencies similar to that of broadband noise.

A measure of the 'phase-noise' performance of the oscillator is to compare the carrier signal to the resulting sidebands and the oscillator noise sideband level is normally plotted in terms of power in a one hertz bandwidth according to the relation [58]:

\[
\frac{S}{N} = P_{in} + 174 - F - 20 \log \sqrt{\frac{f}{2Q_A f}}^2 + 1 \text{ dB/Hz} \quad (3.37)
\]

where

- \( P_{in} \) = the power level at the amplifier input.
- \( \Delta f \) = offset frequency from carrier \( f_0 \).
- \( F \) = noise figure of the amplifier.
\[ Q = \text{oscillator quality factor} \]
\[ f_c = \text{carrier frequency}. \]

From Eq. (3.37), the oscillator spectral characteristics can be represented as shown in Fig. 3-14, in which the breakpoint B occurs at offset frequency \( \Delta f = \frac{f_c}{2Q} [58/59] \). For frequencies greater than \( \frac{f_c}{2Q} \) from the carrier the noise sidebands are constant in level and \( \frac{S}{N} \) is given by [58]:

\[
\frac{S}{N} = P_{in} + 174 - F \text{ dB/Hz} \tag{3.38}
\]

At frequencies less than \( \frac{f_c}{2Q} \) from the carrier, the noise sidebands increase at 20 dB/decade towards the carrier.

3.6.2 Frequency Stability of LC and Crystal Oscillators

In LC oscillators, the circuit components particularly transistors change their characteristics with age, temperature, voltage, etc [33]. Hence, their long and medium-term frequency stabilities are poor and a trimming process is normally required to adjust the operating frequency. However, specially designed LC-oscillators can achieve high stability and frequency drifts of \( 2.8 \times 10^{-7} \) per day have been reported [40]. In LC-voltage controlled oscillators (LC-VCOs), the presence of variable reactances further degrades oscillator stability.

Due to the importance of LC-VCO phase noise in multi-channel communications systems it is necessary to define this mathematically. It can be shown that the phase-noise of an LC-VCO is given by [60]:

\[ \text{Phase-noise} \text{ of LC-VCO} \]
\[ S = 10 \log \left[ \frac{f_0^2 KT_0 \left( \frac{1}{Q_L} + \frac{1}{Q_C} \right) \sqrt{\frac{L}{C}}}{V_s^2 (\Delta f)^2} \right] \text{ dB/Hz} \] (3.39)

where

\[ f_0 = \text{carrier frequency} \]
\[ K = 1.38 \times 10^{-23} \text{J/K} \ldots \text{Boltzmann's constant.} \]
\[ T_0 = 290 \text{ Kelvin (}17^\circ\text{C)} \ldots \text{standard ambient temperature.} \]
\[ Q_L = \text{quality factor of the inductor alone and is given by } \frac{1}{G_L \omega_L}, \text{ where } G_L \text{ is the inductor's own conductance.} \]
\[ Q_C = \text{quality factor of the capacitor alone and is given by } \frac{\omega_C}{G_C}, \text{ where } G_C \text{ is the capacitor's own conductance.} \]
\[ V_s = \text{rms voltage of the oscillator output.} \]
\[ \Delta f = \text{offset frequency from carrier.} \]

In crystal controlled oscillators the frequency is essentially determined by the crystal, and not by the rest of the circuit. Crystals are available with high values of Q (typically \(3 \times 10^3\) to \(1 \times 10^6\) [42]). This plus the fact that the characteristics of Quartz are extremely stable with respect to time and temperature [61] accounts for the exceptional frequency stability that can be obtained with oscillators incorporating crystals. For frequency and time standards, crystal oscillators have been built with frequency drifts less than 1 part in \(10^{10}\) per day [44]. However, factors such as poor cleanliness and contamination of the crystal surface, poor material control of the electrodes or the degree of moisture of the air or gas trapped inside a crystal holder after encapsulation will bring about excessive ageing. Also the failure
to remove surface strains and mounting assembly stresses will also cause drift. Special mounting and encapsulating techniques are required to reduce these effects [61].

The variation of frequency with temperature for a given crystal is dependent on a number of factors, the most important of which is the angle at which the crystal plate is cut in relation to the three main axes of the crystal. AT-cut Quartz crystals are the most temperature stable types and are widely used for such applications. The minimum obtainable frequency change over a wide temperature range depends on the accuracy to which the angle of cut can be achieved. When there is a demand for a low frequency deviation over a wide temperature range, eg. \( \pm 2 \) pp \( 10^7 \) drift over \(-40^\circ C \) to \(75^\circ C\), a means of temperature compensation is required. This can be achieved by the use of a temperature controlled oven or electronically compensated crystal oscillator circuit [62] in which the reactive load of the oscillator presented to the crystal can alter inversely as the crystal reactance alters with temperature so that frequency changes due to temperature drifts can be compensated for.

3.6.3 Frequency Stability of SAW Oscillators

Following the conventional approach, the frequency stability of SAW oscillators is classified into three regions: long, medium and short-term stabilities. Long term ageing has so far been a major problem. It is possible that SAW devices are subject to ageing due to the acoustic energy being confined to the substrate surface which is liable to more contamination than the bulk of the crystal [63], and it has been experimentally observed that ageing rates are
considerably affected by cleaning and packaging \cite{38/64}. Other parameters which may also affect ageing are the type of surface polish and the quality of the Quartz material.

Improvements in long-term stability (ageing) have occurred, largely due to better packaging techniques. Cleaning and sealing techniques similar to those used with bulk wave resonators have recently produced oscillators with ageing rates as low as \pm 0.25 ppm/month \cite{38}. Medium-term stability of SAW oscillators is mainly determined by the temperature characteristics of the SAW material. The most common material for a SAWO is ST-Quartz, the delay variation with temperature of which is shown in Fig. 3-15. Here the frequency varies with temperature according to the relation \cite{65}:

\[ f = f_0 \left[ 1 - a (T - T_0)^2 \right] \] \hspace{1cm} (3.40)

where

- \( f \) = the operating frequency.
- \( f_0 \) = the maximum frequency occurring at temperature \( T_0 \).
- \( T \) = temperature
- \( T_0 \) = the turnover temperature.
- \( a \) = second order thermal coefficient of the material, \( = 3 \times 10^{-8} \), its exact value depends on the angle of rotation \cite{66}.

The maintaining amplifier contributes to the frequency/temperature dependence of the oscillator in two main ways \cite{67}:

Firstly, it increases the frequency drift as the temperature goes far from its turnover value resulting in increasing convex curvature of the parabolic temperature characteristics of the SAW material alone. Secondly, it changes the value of the turnover
temperature.

The search for SAW materials with improved temperature behaviour is continuing actively [12, 15]. SiO₂/LiTaO₃ overlay structures offer better temperature performance when compared with ST-Quartz. However, it requires complicated fabrication techniques. Certain cuts of Berlinite have been reported to exhibit temperature characteristics which are also better than Quartz, with the advantage that it is not a composite structure and therefore does not require a complicated fabrication procedure as it is the case for SiO₂/LiTaO₃.

In addition to new materials, alternative approaches to improve the temperature stability of SAW oscillators are possible. One method is to oven the oscillator, where its temperature can be held around \( T_0 \). Another approach is to control the SAW oscillator by a high stable crystal oscillator through a phase-lock technique [68/69]. In applications where the crystal reference oscillator is an integral part of the system, eg. frequency synthesisers, the phase-lock approach can be very useful [70]. Here, the locking technique will compensate for drifts due to temperature and also for ageing, because such frequency drifts, normally slow and within the phase-locked loop bandwidth, are automatically corrected by the loop. Moreover, this approach will improve the phase-noise characteristics of the oscillator as described in Chapter 4. The phase-locking technique has been implemented in all systems reported in this thesis.

In relation to short-term stability (phase noise), SAW oscillators are classified into two groups, resonators and delay-stabilized oscillators. SAW resonators can operate with Q values
comparable with that of bulk crystal resonators but with UHF frequencies. Therefore it is possible to realize SAW resonator controlled frequency sources which are capable of offering improved phase-noise performance at high frequencies. As the SAW resonator Q is defined in terms of an equivalent circuit which has components analogous to that of bulk crystals, its phase-noise characteristics can be obtained using Eq. (3.37). On the other hand, for delay stabilized SAW oscillators an expression has been achieved for 'phase-noise' in terms of the delay line parameters given by [65]:

\[ SSB \text{ FM Noise} = 10 \log \left( \frac{4G^2KT\omega_0^2}{(\omega_0\tau)^2 P_o (\Delta\omega)^2} \right) \text{ dB/Hz} \quad (3.41) \]

where

- \( G \) = the amplifier gain
- \( K \) = Boltzmann's constant (= 1.38 x 10^{-23} \text{J/K})
- \( T \) = ambient temperature (K)
- \( F \) = noise figure of the amplifier
- \( \omega_o \) = operating frequency (carrier)
- \( \tau \) = SAW delay line length (sec)
- \( P_o \) = output power
- \( \Delta \omega = [2\pi(\Delta f)] \) offset from carrier frequency \( f_o \).

Equation (3.41) can be re-arranged in the form:

\[ 10 \log \left( \frac{G^2KT F f_o^2}{\frac{Q^2}{Q_o} P_o (\Delta f)^2} \right) \]  \quad (3.42)

'Q' in Eq. (3.42) is equal to \( \pi L \) as defined in Eq. (3.22) where \( L \) is the SAW delay line length in wavelength (\( \lambda \)).
Depending on the operating conditions, SAW delay line controlled oscillators can be designed to give either high Q's ($\sim 10^4$) with limited frequency deviation capability or low Q's ($\sim 10^2$) where frequency deviations up to 1% are possible.

SAW oscillators designed with Qs $\geq 10^3$ exhibit improved phase-noise performance when compared to their competitors, the LC-oscillators, at the same power level and operating frequency, due to the difficulty in design LC-VCOs with Qs higher than $10^3$. This conclusion is reinforced by experimental results presented in Section 6.2.
FIGURE 3-13. Simple oscillator model.

FIGURE 3-14. Oscillator 'phase-noise' presentation.
FIGURE 3-15. Frequency temperature characteristics of ST Quartz ($\theta = 42.75^\circ$).
Radio traffic in the VHF/UHF frequency bands is increasing very rapidly. Large numbers of channels, closer channel spacing, improved frequency stability, and fast channel selection are consequently required. To meet these requirements, frequency synthesisers are now being widely used as transmitter exciters and receiver local oscillators. These are replacing systems which utilized continuous tuning, one disadvantage of which was the lack of fast accurate tuning of a desired channel.

Frequency synthesisers are capable of deriving discrete frequencies in a particular radio frequency band from a high stability reference source. The stability of this source is transferred to all the output frequencies [71].

Initial designs of frequency synthesisers used a method of crystal switching combined with mixing to provide the multi-channel operation required and mechanical switches were used to select the desired frequency channel. Advances in IC technology and the availability of varactor tuners have made possible the realization of a new generation of frequency synthesisers which eliminate the need for many crystals and provide automatic channel selection in response to a logic word [72]. IC technology also offers great advantages in terms of size and cost. Complete multi-channel synthesisers operating at low frequency fabricated on a single chip have been designed [73].
Digital synthesizers offer system flexibility as they are capable of being programmed externally through the use of computer techniques and frequency selection can be easily controlled from a central command station.
4.2 DIRECT AND INDIRECT FREQUENCY SYNTHESISERS

Presently, two basic methods exist by which a signal may be synthesised. These are 'direct' and 'indirect' \([71]\). The direct method relies upon multiplication and division of the reference signal to produce a set of output frequencies. The indirect method relies upon the use of programmable phase-locked loops (PLL) to provide the multi-channel operation required.

Direct synthesisers are complex and expensive, but they have the advantage of fast switching between the output frequencies. Indirect synthesisers are usually less complex and less expensive but they have drawbacks in applications where fast switching between channels is required due to the 'settling time' required by the phase-locked loop when it is subject to channel switching.

An example of a direct frequency synthesis technique \([74]\) is shown in the simplified block diagram of Fig. 4-1. An ultra stable crystal oscillator is followed by a harmonic generator to produce multiples of the reference signal. A set of bandpass filters followed by amplifiers is then used to select the required harmonics. These harmonics of the reference are then fed into a switch matrix. According to a digital command to this switch matrix, two output frequencies \((F_1\text{ and } F_2)\) are selected as shown. \(F_1\) is fed into one part of a mixer and \(F_2\) is divided by \(R\) then filtered and fed into the second part of the mixer. The output from the mixer is then filtered and amplified to form the required synthesiser output which is given by \(F_{\text{out}} = F_1 + \frac{F_2}{R}\). A large number of programmable frequencies can be obtained from this synthesiser depending on the number of harmonics and the value of \(R\). The switching time between any two of the possible output
frequencies depends on the response time of the switch matrix alone, because any required frequency $F_1$ or $F_2$ is always available at the switch matrix input. The response time of the switch matrix can be designed to be very short, typically microseconds.

Due to the complexity, cost and size direct synthesizers are used only when there is a requirement for a very fast switching time ($\ll 100 \mu \text{sec}$) [74].

'Indirect' technique is the other approach to frequency synthesis. Fig. 4-2 shows a block diagram of a single loop indirect frequency synthesiser. The output of a voltage-controlled oscillator (VCO) is divided and locked to a highly stable crystal oscillator through a phase-locked loop. The design of this loop determines the performance of the synthesiser. The required output frequency is defined by a logic word into the programmable divider as shown. The loop is locked to an output frequency $f_0$ located within the VCO pull range. In this state, the input frequency $f_2$ to the phase-detector (PD) is equal to the reference frequency $f_1$. Any other desired frequency can be selected by proper digital command into the programmable divider. This will result in the input frequency $f_2$ being different from the reference frequency $f_1$ and a correction signal is then generated at the PD output. This correction signal is filtered to produce a d.c. control voltage which is applied to a varactor-tuning circuit in the VCO. The output frequency of the VCO is then changed to a value at which the relation $f_2 = f_1$ is satisfied and the loop automatically locks to the new output frequency. Here the 'switching time' between the output frequency channels is dependent on the response of the loop. This is normally very slow.
compared to the direct method of frequency synthesis.

The advantages of low cost, small size and improved phase-noise performance (see Section 4.6) result in 'indirect' frequency synthesis being used in the majority of applications where very fast switching speeds are not required.
FIGURE 4-1. Typical form of direct frequency synthesis system

\[ f_0 = F_1 + \frac{F_2}{R} \]

FIGURE 4-2. Basic configuration of indirect frequency synthesiser.
4.3 THE PHASE-LOCKED LOOP (PLL)

4.3.1 PLL Basic Configuration

A block diagram of a simple phase-locked loop is shown in Fig. 4-3a. This is a closed loop electronic servo consisting of a voltage controlled oscillator (VCO), phase-detector (PD) and a loop filter. The output of the VCO locks on and tracks the input reference signal. The loop is locked when there is no phase-error between the input signals to the phase-detector. If a change of phase takes place, then the phase-detector produces an output proportional to the phase-difference between its two inputs. This phase-error output goes to the loop low-pass filter, which may be followed by an error amplifier. The tasks of the loop filter are:

i) attenuation of fast changes in phase-error due to noise in the input signal, ie. it provides a short-term memory for the PLL and ensuring a rapid capture of the signal if the system is thrown out of lock due to noise transients.

ii) smoothing out the high-frequency ripple component of the PD output, which helps to reduce the residual FM on the VCO output.

The d.c. error voltage from the filter changes the frequency of the VCO in the proper direction to maintain the phase-lock.

The phase-locked loop is characterized mathematically by the same equations that apply to other conventional feedback control systems. Referring to Fig. 4-3b, the basic loop equation is given by:

\[
\frac{\phi_c(s)}{\phi_r(s)} = \frac{G(s)}{1 + G(s)H(s)}
\]  (4.1)
where
\[ \phi_o(s) = \text{output phase} \]
\[ \phi_r(s) = \text{input reference phase} \]
\[ G(s) = \text{forward gain transfer function} \]
\[ H(s) = \text{feedback gain transfer function} \]

The loop components transfer functions are shown in Table 4-1, from which Eq. (4.1) becomes

\[ \frac{\phi_o(s)}{\phi_r(s)} = \frac{K}{s} \times F(s) \frac{1}{1 + \frac{K}{s} \times F(s)} \]  

(4.2)

where \( K \) is the gain product of the VCO and the phase-detector \( (K = K_o K_d) \).

Equation (4.2) can be reduced to the form

\[ \frac{\phi_o(s)}{\phi_r(s)} = \frac{1}{1 + \frac{s}{K F(s)}} \]  

(4.3)

In the steady state:

\[ \frac{\phi_o(s)}{\phi_r(s)} (t = \infty) = \lim_{s \to 0} \left[ \frac{1}{1 + \frac{s}{K F(s)}} \right] = 1 \]  

(4.4)

where

\[ t = \text{time}. \]

Which means that during lock \( \phi_o(s) = \phi_r(s) \) without any error.

4.3.2 The Digital PLL

A single loop digital frequency synthesiser is formed when a programmable divider (see Section 4.4) is inserted into the
feedback path of the phase-locked loop as shown in Fig. 4-4. The reference signal $f_r$ is derived from a highly stable crystal-controlled oscillator. The division ratio $N$ of the programmable divider and the frequency of the reference signal $f_r$ are chosen so that the VCO output frequency $f_o$ satisfies the relation:

$$f_o = N f_r \quad (4.5)$$

where $f_o$ is the desired output frequency.

In this loop the inputs to the phase-detector are the reference signal $f_r$ and the output from the programmable divider $f_o/N$. Any phase change between these two inputs causes the phase-detector to produce a voltage proportional to this change. The voltage from the PD output after filtering is used as a control signal for the VCO to pull its frequency in the proper direction so as to satisfy Eq. (4.5). Varying $N$ changes the output frequency in increments equal to the reference frequency. This means that for this loop the spacing between the output frequencies is

$$f_{ch} = f_r \quad (4.6)$$

where

$$f_{ch} = \text{channel spacing}$$

Referring to Fig. 4-4, the digital PLL can also be characterised by Eq. (4.1), but with $H(s) = \frac{1}{N}$. Hence, Eq. (4.2) for digital PLL takes the form

$$\frac{\Phi_o(s)}{\Phi_r(s)} = \frac{K}{s} \frac{F(s)}{1 + \frac{K}{s} F(s) \cdot \frac{1}{N}} \quad (4.7)$$
Dividing both sides by \( N \) and defining \( \phi'_o = \frac{\phi_o}{N} \) and \( K' = \frac{k}{N} \), then Eq. (4.7) becomes

\[
\frac{\phi'_o(s)}{\phi_T(s)} = \frac{K' \cdot F(s)}{s + K' \cdot F(s)} = \frac{1}{1 + \frac{s}{K' \cdot F(s)}}
\]  

which takes the same form as Eq. (4.3) with reduced gain and output phase by a factor of \( N \).

4.3.3 Type and Order of the PLL

The type of feedback control system is determined by the number of pure integrators \( \left( \frac{1}{s} \right) \) in the loop \([77] \). In phase-locked loops, the VCO is an integrator as its phase versus voltage is given by \( \frac{K_0}{s} \) (where \( s \) in the denominator converts the frequency characteristics of the VCO to phase, \( \phi = \int 2\pi f \, dt \)). If a lag or lag-lead loop filter is used then a type I loop is realized. If an integrator-filter is used, then the loop will contain two integrators and is classified as type II.

The order of a system refers to the highest degree of the polynomial expression given in Eq. (4.9) below, which is termed as the characteristic equation (CE) of the system \([77] \):

\[
CE = 1 + G(s) \cdot H(s) = 0
\]  

Referring to Equations (4.8) and (4.9), it is clear that the order of the loop is determined by the transfer function of the filter \( F(s) \). When no filter is used, \( F(s) = 1 \), then a first-order system results. In practice however, a filter is always required to achieve proper loop operation. With the use of a filter, a higher order system results.

An improved type II PLL is realized with the use of what is
called a type II phase-detector. This phase-detector is complex in design, but its operating characteristics are very useful, especially for digital loop synthesisers [78].

Type II loops incorporating type II phase-detectors are the most desirable approach for frequency synthesis applications for a number of reasons [77/78]. The a.c. components from the PD output, if not suppressed, are riding on the d.c. control voltage to the VCO and modulate its output frequency. Loops with type I PD require sophisticated filters to suppress these a.c. components because their energy is large. Such filters, with their high attenuation put a limitation on the switching speed of the synthesiser. The output from a type II PD is in the form of a very small energy pulse which can easily be smoothed by a simple filter. So, improved VCO spectral purity and loop switching speed are obtained with the type II design approach. A type II PLL maintains a steady state zero error for all operating conditions. Input signals \( f_r \) and \( f_o/N \) to the phase-detector are equal in both phase and frequency (see Table 4-2). This can provide phase coherency in the receivers, a desirable feature for some applications. A type II PLL allows the coverage of the whole VCO pull-range, which is an important property for frequency synthesis applications as it permits a full exploitation of all the frequency channels available within the VCO bandwidth.

4.3.4 PLL Design

For frequency synthesis applications, important PLL design parameters are: (i) natural frequency \( \omega_n \); (ii) loop bandwidth \( \omega_{3-dB} \); (iii) loop lock and capture ranges; (iv) stability factor
(M_p) and (v) settling time \( t_s \). These parameters are discussed below:

i) Natural frequency \( \omega_n \):
This is the characteristic frequency of the loop and may be defined \([79]\) as the frequency for which an underdamped loop gives the maximum output phase error swing.

ii) Bandwidth \( \omega_{3-\text{dB}} \):
A loop property related to the natural frequency and stability factor. It describes the effective bandwidth of the input signal. Noise and signal components outside this band are greatly attenuated. To reduce internal loop noise (eg. inherent VCO noise and noise due to mechanical shocks and vibrations), a wide loop bandwidth is required as any frequency variation at the output is compensated for by a change at the VCO control input as long as the speed of this change lies within the bandwidth of the loop. Also the loop bandwidth must be well defined when frequency modulation is required. FM can be accomplished by applying a modulation signal superimposed upon the control voltage of the VCO at frequencies beyond the loop bandwidth \([80]\). Hence this bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components and causing the VCO to deviate in frequency.

iii) Lock and Capture Ranges:
These are important loop parameters which have to be considered in PLL design. 'Lock-range' is defined as the range of input frequencies over which the loop will remain in lock. 'Capture-range' is the range over which the loop can acquire lock \([79]\). Although
the loop will remain in lock throughout its lock-range, it may not be able to acquire lock at the tracking extremes. In a type I PLL the capture-range is smaller than the lock-range depending on the degree of filter attenuation [81], while in a type II PLL employing a type II phase-detector and integrator filter lock-range is equal to capture-range independent of the filter.

iv) Stability factor:
In a PLL, the stability factor refers to the ability of the loop to response quickly to an input frequency step without excessive overshoot. One of the measures of this factor, which can be seen from the closed-loop frequency response, is the ratio of the feedback phase signal $\phi'_0$ to the reference signal $\phi'_r$, $M_P = \frac{\phi'_0}{\phi'_r}$. A value of $M_P = 1.3 - 1.5$ indicates satisfactory loop stability and time domain performance [82].

v) Settling Time:
This is defined [83] as the time required for the loop response to a unit-step input to reach and remain within a specified percentage (~5-10%) of its final order.

Figure 4-5 shows in the time and frequency domain a typical response of a closed phase-locked loop with the natural frequency, loop bandwidth, stability factor and settling time defined schematically. These loop parameters are related to each other. This relationship is determined mathematically in accordance with the loop type and order. They are all normally expressed in terms of loop gain and filter elements.

The loop synthesiser design procedure begins when the VCO is chosen. This determines the output frequency operating range.
The channel spacing is decided according to the system application. Knowing the VCO operating frequency and the required channel spacing leads to the design of dividers (both fixed and programmable). A phase-detector is then chosen. Once the VCO, PD and counters are fixed, each having its own transfer function, the only variable left for optimization is the loop filter.

Depending on the PD in use and type and order of the loop, many loop filter configurations are possible. Some of these are given in Table 4-3. The first two filters are common in practice and are suitable for use with normal phase-detectors which give a voltage output. Analysis and design of PLLs incorporating such filters are found in the literature. A good design example for a practical avionic loop synthesiser using a lead-integrator filter is given in reference (84).

Recently more developed designs of phase-detectors have appeared. These phase-detectors are of type II and give a current output drive rather than voltage output. A suitable filter for use with such phase-detectors is the lead-lag integrator filter (shown also in Table 4-3). Type II PLLs incorporating current-output phase-detector and lead-lag integrator filter has been studied by Atkinson and Allen [82]. A more comprehensive study has also been carried out by Thrower [85], in which he produced a design, tables and graphs together with a design procedure to calculate the filter elements for optimum loop performance. This procedure has been followed in the design of synthesis
typeIIreported in Chapter 7 as they were based on current-output phase-detectors.
FIGURE 4-3. (a) The basic phase locked loop.

(b) Equivalent feedback network of the loop shown in (a).
<table>
<thead>
<tr>
<th>Element</th>
<th>Transfer Function</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCO</td>
<td>$K_o/s$</td>
<td>$K_o$ is the slope of the oscillator frequency/voltage characteristic in rads per sec. per volt.</td>
</tr>
<tr>
<td>Divider</td>
<td>$1/N$</td>
<td>$N$ is division ratio.</td>
</tr>
<tr>
<td>Phase-detector</td>
<td>$K_d$</td>
<td>$K_d$ is slope of PD voltage/phase characteristic in volts/radian.</td>
</tr>
<tr>
<td>Filter</td>
<td>$F(s)$</td>
<td>Transfer function depends on particular filter used.</td>
</tr>
</tbody>
</table>

**Table 4-1**

Transfer functions of various PLL components
FIGURE 4-4. The basic configuration of a digital phase-locked loop.

Table 4-2. Steady state phase errors for type I and type II PLLs
\( \omega_n = \text{natural frequency} \)

\( \omega_{3\text{dB}} = \text{3 dB bandwidth of the loop} \)

\( \omega_c = \text{cut-off frequency} \)

**FIGURE 4-5. Typical time and frequency response of a closed phase-locked loop**
<table>
<thead>
<tr>
<th>Filter</th>
<th>Type</th>
<th>Transfer function</th>
<th>Time constants</th>
<th>Bode diagrams</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Lag/Lead Diagram" /></td>
<td>Lag/Lead</td>
<td>$\frac{I + ST_2}{I + ST_1}$</td>
<td>$T_1 = C_1(R_1 + R_2)$, $T_2 = C_1 R_2$</td>
<td><img src="image2.png" alt="Gain" /> <img src="image3.png" alt="Phase" /></td>
</tr>
<tr>
<td><img src="image4.png" alt="Integrator and Lead Diagram" /></td>
<td>Integrator and Lead</td>
<td>$\frac{I + ST_2}{ST_1}$</td>
<td>$T_1 = C_1 R_1$, $T_2 = C_1 R_2$</td>
<td><img src="image5.png" alt="Gain" /> <img src="image6.png" alt="Phase" /></td>
</tr>
<tr>
<td><img src="image7.png" alt="Integrator and Lead Diagram" /></td>
<td>Integrator and Lead</td>
<td>$\frac{1}{sC_1} \cdot \frac{1 + ST_2}{1 + ST_3}$</td>
<td>$T_1 = C_1 R_1$, $T_2 = R_2(C_1 + C_2)$, $T_3 = C_2 R_2$</td>
<td><img src="image8.png" alt="Gain" /> <img src="image9.png" alt="Phase" /></td>
</tr>
</tbody>
</table>

**TABLE 4-3.** Transfer function and Bode diagrams of various filter networks
4.4 VHF/UHF SYNTHESISER REQUIREMENTS

4.4.1 The Programmable Divider

In digital PLL synthesisers, the programmable divider N is used to control the VCO output frequency. Fig. 4-6 shows a 3-stage programmable divider. The first stage (A) will count at the highest frequency (the input frequency to the counter) and will correspond to the least significant digit. To achieve direct frequency programming this stage must satisfy certain division radix requirements depending on the channel spacing required (see 4.4.3). Other counter stages are normally arranged in cascaded decades. Each stage will count from a pre-set state down to state 0 (in case of down counters). The programmable counter operation can be explained by the following example. Suppose it is required to divide by \( N = 476 \) (this figure is applicable to the UHF synthesiser presented in Chapter 7). Assuming that all stages are decadic, then counters 4, 7 and 6 are pre-set into stages C, B and A respectively. After 6 input clock pulses, stage A will reach state 0, but no recognition will take place as both stages B and C are not at state 0. Stage A will therefore move to state 9 on the next input clock and at the same time produces an output clock pulse to stage B. Stage B then will move to state 6. Stage A continues to divide by 10, producing a clock pulse to stage B, so that 69 pulses later both A and B are on state 0. The next input pulse will cause A and B to move to state 9 and C to move to state 3. After another 399 pulses, during which time stages A and B are dividing by 10, all three stages will be on state 0, giving an output pulse, and the recognition gate allows the present information to return the divider to the start of the
cycle again where another output pulse will be produced. The repetition rate of these output pulses is given by:

\[ f_N = \frac{f_{\text{in}}}{N} \]  \hspace{1cm} (4.10)

where

- \( f_N \) = output frequency of the counter
- \( f_{\text{in}} \) = input frequency to the counter
- \( N \) = the counter division settling.

4.4.2 Prescaling

For technical and economical reasons, programmable division functions are achieved by using standard TTL or CMOS ICs. The maximum operational speed of these logic circuits is well below the required output frequencies from the VCO in a PLL VHF/UHF frequency synthesiser. So it is required to reduce (prescale) the VCO output frequency to a value which can be handled by TTL or CMOS logic. To achieve this, one of the following techniques can be used: (i) Heterodyne down conversion; (ii) fixed prescaling and (iii) variable prescaling.

i) Down Conversion:

In this method [86] an offset oscillator is employed to 'mix-down' the VCO frequency \( f_0 \) (see Fig. 4-7) and the desired output frequency \( f_K \) is obtained after suitable bandpass filtering, \( f_K \) is given by

\[ f_K = f_0 - f_{\text{off}} \]  \hspace{1cm} (4.11)

where

- \( f_{\text{off}} \) = the output frequency of the offset oscillator.
With this arrangement, the loop comparison frequency \( f_{\text{comp}} \) and the output frequency \( f_o \) are given by:

\[
f_{\text{comp}} = \frac{f_o - f_{\text{off}}}{N}
\]

(4.12)

and

\[
f_o = N \times f_{\text{comp}} + f_{\text{off}}
\]

(4.13)

From Eq. (4.13) it is evident that the comparison frequency is equal to the required channel spacing. Hence the loop bandwidth is uncompromised and optimum PLL performance can be achieved. However, a major disadvantage of this technique is that the addition of the offset frequency will reduce the achievable frequency stability of the VCO as its output will be contaminated by spurious beat and sum frequencies. Another disadvantage is the need for another oscillator. With the advances that have taken place in IC technology, the heterodyne down conversion method, with its serious disadvantages of degraded output spectral purity and need for multiple oscillators, becomes unattractive.

The present trend is towards the use of high-speed ECL dividers to achieve the VCO prescaling function as explained in the following prescaling techniques.

ii) Fixed Prescaling:

A block diagram for a digital PLL with a fixed prescaler \([87]\) is shown in Fig. 4-8. The VCO output is prescaled by a division factor 'M' to a value that can be handled by the IC programmable counter (N). The reference frequency \( f_r \) is nominally equal to the channel spacing \( f_{\text{ch}} \). However, where a prescaling divider is employed, the value \( f_r \) must be reduced by a division ratio 'M', hence:
When the loop is locked, the input frequencies to the phase-detector are equal:

\[ f_r = f_N \]  \hspace{1cm} (4.15)

\( f_N \) is the output from the programmable counter and is equal to the comparison frequency \( f_{\text{comp}} \).

Using Eq. (4.14), \( f_N \) is then related to the channel spacing by:

\[ f_N = \frac{f_{\text{ch}}}{M} \]  \hspace{1cm} (4.16)

But

\[ f_N = \frac{f_o}{(M \times N)} \]  \hspace{1cm} (4.17)

Then the VCO output frequency \( f_o \) is related to \( f_r \) by:

\[ f_o = M \times N \times f_r \]  \hspace{1cm} (4.18)

\( N \) is defined in the programmable counter by an external frequency control code. It is normally set in integer steps and consequently \( f_o \) can only be altered in steps of \( M f_r \).

The programmable divider for the prescaled PLL system has to have the same number of stages as in the basic PLL (unprescaled) even though its maximum frequency of operation has been lowered by a factor of \( M \). When comparing the prescaled PLL with the basic PLL, it is clear that the comparison frequency, which imposes an upper limit to the bandwidth of the PLL, has been reduced by a factor of \( M \). This puts a limitation on the 'settling time' \([82]\) of the loop and also on the short-term stability of the synthesiser output \([78]\).
Hence to achieve a given channel spacing in $f_o$ without compromising the comparison frequency, the smallest possible value for $M$ should be used.

iii) Variable Prescaling:
As the VCO operating frequency extends upward in the UHF band, the amount of prescaling required becomes excessive and for a given channel spacing $f_{ch}$, the comparison frequency $f_{comp}$ will become very small (see Eq. 4.16). This will lead to a synthesiser design which may not give a satisfactory tuning time and adjacent channel suppression due to loop performance degradation in terms of 'settling time' and 'phase-noise'. To overcome these problems a variable prescaling (sometimes called a dual-modulus prescaling) technique is used. With this technique, it is possible to have effective programmable division at the variable prescaler input frequency, with the actual programmable dividers operating at the output frequency of the variable prescaler. This can be achieved by the use of a high speed divider which can divide by 'P' and 'P+Q', according to the logic state of a programming input.

A block diagram for a PLL based on dual-modulus prescaling technique is shown in Fig. 4-9. The output of the variable prescaler 'A' drives two programmable dividers in parallel. These two dividers are programmed to 'B' and 'N'. The 'B' counter and the variable prescaler 'A' are interconnected in such a way that in a complete count cycle of B, the prescaler divides by 'P+Q'. At the end of the preset count 'B' the programming counter 'B' gives a command to the variable prescaler 'A' to revert its division ratio to 'P'. The 'B' counter is connected also to the
'N' counter so that when 'N' completes its count cycle 'N'
both B and N counters reset. It should be noted that at the end
of the count cycle '+B', the output of the counter B goes high
and remains high so inhibiting any further input clock pulses until
the end of the complete variable divider, N count cycle.

Fig. 4-10 shows the waveforms of the dividers A, B and N
from which it can be seen that this prescaler system divides by
'P+Q' for 'B' counts and by 'P' for 'N-B' counts. Then the whole
programmed count is given by:

\[ R = (N - B)P + A(P + Q) \]  
\[ R = NP + BQ \]

In most cases Q = 1. Hence the output frequency \( f_o \) is given by:

\[ f_o = (NP + B) f_{comp} \]

If B is incremented by one, the output frequency changes by
'\( f_{comp} \)'. On other words, the channel spacing is equal to the
comparison frequency. Hence the loop bandwidth is kept uncom-
promised resulting in an improved PLL design in terms of 'tuning
time' and 'phase-noise'. For continuous programming, N is normally
programmed in unity steps. Therefore, referring to Eq. (4.21),
it can be seen that the upper limit to the B counter is '+P'. So
the B counter must be capable of counting all numbers up to and
including (P-1), or:

\[ B_{max} = P - 1 \]

For this system to work, the 'B' counter must fill up before
the 'N' counter (see Fig. 4-10). This means that N must be higher
in value than \( B, N > B \). But \( B_{\text{max}} = P - 1 \) (Eq. 4.22). Therefore
\[
N_{\text{min}} = P \tag{4.23}
\]

Thus the minimum possible division ratio below which the 'variable prescaler' technique will not function is given by:
\[
R_{\text{min}} = N_{\text{min}} P + B_{\text{min}}
= P \cdot P + 0
\]
or
\[
R_{\text{min}} = P^2 \tag{4.24}
\]

This minimum division ratio puts a limit on the lowest VCO frequency which can be used with such a prescaling system. Using Eqs. (4.21) and (4.24), this frequency is:
\[
f_{\text{low}} = P^2 \times f_{\text{comp}} \tag{4.25}
\]

### 4.4.3 Division Radix Requirements

The output frequency of a synthesiser is frequently set from a thumbwheel or rotary switches. Each stage of the programmable divider is controlled from its own switch. Direct switch programming is possible when the channel frequency spacings are decadic. However, if the channel spacing \( f_{\text{ch}} \) is not decadic, then the first stage of the programmable divider must satisfy a certain division radix \( R_1 \) given by [89]:
\[
R_1 = \frac{10^P}{f_{\text{ch}}} \tag{4.26}
\]

where \( P \) is an integer.

A non-decadic channel spacing of, say, 12.5 KHz, requires \( R_{1\text{min}} = 8 \). This 'division radix' requirement also applies to the
variable prescaler. The basic radix of the variable prescaler must satisfy Eq. (4.26) for direct programming to be obtained. However, the prescaler is usually designed with a 'basic modulus' larger than \( R_{\text{min}} \) to obtain enough prescaling. In the case where 12.5 KHz channel spacing is required at VHF/UHF frequencies, a variable prescaler with moduli 80 and 81 would be required. This will divide the VCO frequency down to a value suitable for TTL or CMOS logic and at the same time satisfy Eq. (4.26).

### 4.4.4 Side-Step Requirement

Communication digital frequency synthesizers are normally employed in equipment operating in a transmit/receive mode [84]. During the transmitting mode, the synthesizer operates at a certain frequency \( f_T \) covering a range \( \Delta f \) to provide the multi-channel requirements. In the receiving mode the synthesizer, acting as a local oscillator, operates at a frequency \( f_R \) which when mixed with the received signal, provides the radio IF frequency (side step frequency). One possible synthesizer frequency allocation for a positive side step is illustrated in Fig. 4-11, from which \( f_R \) is given by:

\[
F_R = F_T + IF
\]

For this type of frequency allocation, the VCO bandwidth has to cover a frequency range (BW) satisfying the relation:

\[
BW = IF + \Delta F
\]

Every output frequency channel is selected by a frequency control switch. The position of this switch represents certain digital codes to programme the variable divider for the required division ratio 'N'.
To operate in the same frequency channel in the receiving mode, the division ratio 'N' must be altered by:

$$\Delta N = \frac{IF}{f_{ch}}$$

(4.29)

with the control switch remaining pointing to the selected channel.

The alternation in the variable divider division ratio can be achieved by an 'offset logic' (or side step logic) interconnected to the variable divider building blocks and controlled externally by a $T_x/R_x$ switch. This switch when in the $R_x$ position will actuate the offset logic to change the division ratio to the required value $(N + \Delta N)$ without changing the code from the frequency control switch. This arrangement is possible with a VCO having enough pull range to cover the frequency range given in Eq. (4.28).

In the case of a SAW-VCO based system, the narrow bandwidth of the SAWO results in transmit/receive synthesizers requiring two SAW oscillators separated in frequency by the radio IF. Alternatively, two delay lines could be used, selected by the $T_x/R_x$ switch, which also controls the variable divider IF side step logic. Also multi-frequency SAW oscillators [47/90] may be useful for this purpose.
FIGURE 4-6. A schematic representation of a simple 3-stage programmable divider.

FIGURE 4-7. Single loop digital frequency synthesiser with VCO offset.
FIGURE 4-8. Single loop digital frequency synthesiser with fixed prescaler.

FIGURE 4-9. Digital frequency synthesiser with dual modulus prescaling systems.
Clock In

Output of 2 modulus

Prescaler 'A'

Program output of 'N'

Modulus control
output of 'B'

'B' Counter programmed to 2

'N' Counter programmed to 7

\[ P = 10 \]

\[ \text{Division ratio} = NP + B = 72 \]

FIGURE 4-10. Typical two-modulus wave forms
FIGURE 4-11. Frequency allocation for a positive
side-step two-way radio operation.

\[(VCO \ BW)_{\text{min}} = IF + \Delta f\]
4.5 THE 'GEMINI' SYNTHESER

In single loop synthesisers, the channel spacing (which may be equal to or greater than the comparison frequency) imposes an upper limit on the loop bandwidth. This in turn will result in a limited synthesiser 'switching-speed'.

Some communications applications demand a fast switching speed and hence, for a given channel spacing, a wide loop bandwidth is required. Various schemes have been proposed to achieve this purpose, all at the expense of an increase in complexity. One of the simplest techniques is the 'Gemini' loop [71], the basic form of which is shown in Fig. 4-12. Two fixed frequency inputs are required; \( f_R \), the reference and \( f_1 \), an interpolation frequency. \( f_1 \) is fed to a programmable divider which has the same division ratio as that of the main loop divider. The resultant frequency \( f_1 / M \) is then mixed with the reference \( f_R \). The sum product of the mixer is selected by a bandpass filter and applied to the phase-detector. The comparison frequency at the PD is then

\[
\frac{f_{\text{comp}}}{f_R} = \frac{f_1}{f_R} + \frac{f_1}{M}
\]  

The programmable dividers in the feedback loop and the interpolation section are linked together, hence the output frequency \( f_o \) of the synthesiser is given by:

\[
f_o = M(f_1/M + f_R) = f_1 + Mf_R
\]  

Thus the output frequency can be changed in steps of \( f_R \) by altering the feedback ratio \( M \) as in the single loop synthesiser but the comparison frequency has been increased. This allows an increase in loop bandwidth to a value several times longer than
the channel spacing, permitting a fast switching speed to be achieved. Also the Gemini approach can result in an improved 'phase-noise' frequency source for synthesisers operating at frequencies within the lower UHF band (see Section 4.6).
FIGURE 4-12. GEMINI LOOP.
14.6 PHASE-NOISE PERFORMANCE OF FREQUENCY SYNTHESISERS

In the case of direct frequency synthesisers, the noise characteristics of the output frequency are directly derived from the reference oscillator \([74]\). However, this output is subject to spurious products which result from the mixing processes and noise in amplifiers (see Fig. 4-1). When operation is required at UHF and microwave frequencies, the output of the synthesiser is normally multiplied to give the wanted frequency. This multiplication process causes additional degradation in the phase-noise performance given by \([58]\)

\[
\text{Phase noise degradation} = 20 \log M
\]

where, \(M\) is the frequency multiplication factor.

Referring to Fig. 4-13, curve A shows a typical phase-noise characteristic for a direct synthesiser. The phase noise decreases as the offset frequency from carrier increases following the performance of the multiplied reference oscillator until it reaches a point when the phase-noise begins to increase. This increase is due to the thermal noise of the amplifiers and multipliers which governs the phase-noise performance of the synthesiser in this region \([74]\).

'Indirect' frequency synthesisers, employing a voltage-controlled oscillator phase locked to a crystal reference oscillator possess a phase-noise characteristic given by curve B (Fig. 4-13). Close to the carrier their noise is governed by the reference signal, which is degraded slightly due to the multiplication from the operating crystal frequency to the VCO frequency. This good performance is maintained with increasing offset from carrier until the cut-off frequency of the phase-locked loop is approached.
Here, the phase-noise flattens out until the low Q VCO phase-noise curve is reached, whereupon the overall synthesiser phase-noise characteristic follows this curve, [78/91], which decreases with increasing frequency offset. Thus the adjacent channel noise is controlled by the VCO design.

In single loop indirect synthesisers, the comparison (reference) frequency is set by the required channel spacing and hence the loop cut-off must be less than the comparison frequency to provide adequate suppression of control line ripple and noise components. Where the cut-off frequency is low compared to the channel spacing (eg. fixed prescaled PLL) the loop phase-noise performance (as well as its switching speed) will be degraded. This degradation can be avoided in loops designed with bandwidths close to their comparison frequency (eg. loops with no prescaler or with variable prescaling). Further improvement in phase-noise can be realized with loops in which the bandwidth exceeds the upper limit set by the required channel spacing. This can only be done with complex multi-loop indirect synthesisers, one example of which is the Gemini loop described in Section 4.5. However, when adopting such an approach, it should be noted that the phase-noise improvement is dependent on how wide the loop bandwidth is.

In the UHF and microwave frequency regions, if the loop extends beyond a certain limit, the noise sidebands of the synthesiser may increase due to the fact that far away from the carrier the phase noise performance of a multiplied reference is worse than that of free running VCO [91].
FIGURE 4–13. Phase-noise characteristics of direct and indirect frequency synthesizers.
SAW APPROACHES TO FREQUENCY SYNTHESIS

SAW devices, as VHF/UHF signal processing elements, have been the material for many suggestions and configurations to realize a SAW-based frequency synthesiser which may exhibit improved performance, compared against existing synthesisers, in terms of size, cost, ruggedness or phase-noise. One version is the programmable oscillator reported by P Hartemann [90], where a SAW delay line with one input transducer, operating in a certain beam steering mode, and a bank of ten output transducers, positioned according to the beam directions corresponding to their central frequency, has been used. Ten output frequencies in the range (120 - 130) MHz separated by ~0.9 MHz channel spacing and with ~0.7 MHz bandwidths were obtained. Another version which enables closer channel spacing has been reported by Browning et al [92]. This is also a programmable SAW oscillator with single input transducer and multiple output transducers, but its principle of operation is quite different from the above version in that the frequency shift is achieved by changing the SAW path length. (59 - 61) MHz frequency range was covered in 80 equal steps of 25 KHz. However, for this synthesiser to operate properly, a mean must be provided to start the oscillation always at a well defined frequency so that all the subsequent changes are relative to this frequency. Also this programmable oscillator was subject to multi-moding problems, a solution to which has been found [92] with added device complexity and with the SAW device acting as a discriminator instead of a frequency controlling element. Another frequency synthesis approach, reported by Patterson and Hannah [93], was based on the mixing of waveforms from an impulsed SAW linear
FM chirp filters. This system produced 63 channels over 26 MHz bandwidth at 120 MHz operating frequency with very fast switching between its channels. It has potential application in spread-spectrum communication, where rapid frequency hoppers are required. It is difficult with this system to obtain very close channel spacing and its frequency stability is dependent on the SAW chirp filters.

Direct frequency synthesisers require a large number of filters, mixers, RF switches and amplifiers. With SAW devices it is possible to realize good VHF/UHF bandpass filters, which when implemented in direct synthesisers can offer a reduction in cost and size. A SAW filter-based direct synthesiser has recently been reported by Budreau and Carr [94] which was capable of achieving fast frequency hopping among 219 channels covering the frequency band 1369 MHz - 1606 MHz. A compact 16-channel UHF SAW filter suitable also for such application has been reported by Laker et al [95].

The above mentioned SAW-based synthesis ideas, while of interest to certain applications, are unable to meet the requirements of the mobile communications, for which light, less power-consuming synthesisers with very close channel spacing and highly stable well-defined output frequencies are essential.

Currently, communications synthesisers are based on 'indirect' synthesis techniques in which the frequency sources are LC-VCOs. These oscillators, although useful as their pull-range allows them to cover the entire frequency band required for two-way radio, are unstable and difficult to design and manufacture for operation
at a precise frequency. Also the difficulties in mechanically
stabilising the VCO capacitor result in microphony problems. On
the other hand, SAW oscillators, when designed with frequency
control ability, are attractive to communication synthesisers,
where they can offer many advantages as discussed below:

In the previous section it has been shown that the phase-
noise of an indirect synthesiser beyond the loop cut-off fre-
quency is almost entirely governed by the VCO phase-noise
characteristic. This means that the adjacent channel noise is
controlled by the VCO design. Voltage-controlled oscillators
with good phase-noise performance can therefore lead to the
realization of frequency synthesisers with improved spectral
purity and satisfactory adjacent channel suppression (see Fig. 4-14).
Here, SAW oscillators, being capable of operating with high Qs,
are attractive as their phase-noise performance is superior to
that of LC-VCOs currently in use. This conclusion is reinforced
by the results presented in Chapter 6 for experimental oscillators.

Commercial mobile radios are likely to use adjacent channel
working \[96\]. A 70 - 80 dB dynamic range is normally required
\[97\]. The synthesiser noise sideband level is plotted in terms
of power in a one hertz bandwidth and when dealing with radio
operation the synthesiser must achieve a noise sideband level
given by \[98\]

\[
- \left[ 80 + 10 \log \frac{\text{receiver BW}}{1 \text{ Hz BW}} \right] \quad (4.33)
\]

A typical receiver bandwidth is \(3\) KHz, hence according to
Eq. (4.33) the synthesiser noise level must be less than
$115 \text{ dB/Hz} \ (\ -80 - 10 \log \frac{10^3}{1}). \ SAW \ oscillators \ can \ operate \ with \ phase-noise \ level \ below \ this \ figure \ (see \ Section \ 6.2) \ and, \ when \ employed \ as \ VCOs, \ are \ capable \ of \ improving \ the \ noise \ performance \ of \ indirect \ synthesisers \ provided \ that \ wideband \ coverage \ is \ not \ required.

Unlike \ the \ LC-oscillators, \ SAW \ oscillators \ although \ limited \ in \ bandwidth, \ are \ rugged, \ small \ and \ potentially \ attractive \ for \ radiotelephone \ systems \ where \ only \ a \ few \ closely \ spaced \ channels \ must \ be \ covered. \ The \ narrow \ bandwidth \ of \ a \ SAWO \ results \ in \ a \ SAW-based \ transmit/receive \ synthesiser \ requiring \ two \ separate \ SAWOs \ as \ explained \ in \ Section \ 4.4.4.

The \ search \ for \ a \ wideband \ (high \ $K^2$), \ temperature \ stable \ material \ may \ open \ the \ way \ to \ the \ realization \ of \ wideband \ SAW \ oscillators. \ Also \ multi-response \ SAW oscillators [47/90] could be useful for Tx/Rx operation.

SAW oscillators can fundamentally operate in frequency regions up to 2 GHz with high Qs [99]. This is of significance to microwave synthesisers which currently employ low Q frequency sources with tuning difficulties.

In single-channel radiotelephone application, SAW resonator-stabilised oscillators are attractive due to their low insertion loss, high speed spectral purity and FM capability.

It has been found experimentally [36] that SAWOs are completely immune to vibrations, whereas a well-developed voltage-controlled crystal oscillator operating at the same frequency showed a dramatic increase in noise when subject to vibration. This property of SAWOs makes them also attractive for application
in frequency synthesisers now widely used in a large number of equipment, which are subject to mechanical shocks and vibrations such as air-borne, ship-borne and land-mobile radars, automatic direction finders (ADF), electronic-counter measures (ECM), VHF/UHF communications transceivers, etc.

SAW oscillators can operate with high output power (~1w). This helps to reduce the requirements on the power amplifier stage in transmitters.

The major drawbacks of SAWO, its ageing rate and temperature sensitivity (long- and medium-term stabilities), are compensated for in frequency synthesis application following the 'indirect' synthesis technique, where the SAWO is locked to a crystal-oscillator through a phase-locked loop as introduced in the following chapters.
Fig. 4-14 Noise suppression (A) achieved with high Q VCO
CHAPTER V

DESIGN AND PERFORMANCE OF SAW RESONATOR-BASED SINGLE CHANNEL SYNTHESISER

5.1 INTRODUCTION

This chapter describes the design and operation of a single-channel SAW resonator-based synthesiser. The research was carried out to assess the feasibility of incorporating SAW resonators in personal radio-telephones.

The SAW resonator (detailed in Chapter 3) is a new device which is useful as a frequency controlling element in oscillator circuits. The resulting SAW resonator controlled oscillators are attractive for personal radio applications as they offer:

i) fundamental operation at VHF/UHF frequencies.
ii) good phase-noise performance as they are stabilised by a high Q element.
iii) high rf/dc efficiency due to the resonator low losses.
iv) immunity to shocks and vibration.

The addition of a phase-shifting network to the SAW resonator-oscillator allows voltage controlled frequency tuning, thus permitting FM capability and automatic frequency control through phase-lock techniques.
5.2 THE SYNTHESISER MODULE

Existing radio-telephones frequently operate at UHF frequencies. As shown in Fig. 5-1a, the basic frequency source is a bulk-crystal oscillator normally operating in the HF band. Multipliers are used to achieve operation at the required UHF frequencies. This multiplication process is a source of additive noise \[ \text{Eq. (4.32)} \], which results in a degraded output spectral purity. Multipliers are also power consuming elements, putting a limitation on the rf/dc efficiency of the radio-telephone equipment.

In the light of the advantages gained by using SAW resonators, it is feasible to realize pocket-phone equipment with SAW-based frequency sources operating directly at the required frequency. This will lead to simplicity in design and improvements in operation; (i) by eliminating the multipliers; (ii) giving output with improved spectral purity; (iii) immunity to shocks and vibrations and (iv) improved rf/dc efficiency. This latter advantage is of great significance for battery powered equipment.

However, many problems hinder the direct incorporation of SAWOs in radio-telephones. Firstly, the oscillator medium-term (temperature) stability must meet the \( \pm 3 \) KHz UHF radio-telephone requirements \[ \text{Eq. (4.32)} \] over the \(-10^\circ\text{C to } +40^\circ\text{C}\) operating temperature range. This can be achieved with crystal oscillators based on AT cut bulk acoustic wave resonators possessing a crystal cut angle tolerance of \( \pm 1^\circ \) of arc. The most stable SAW oscillators are fabricated on ST cut Quartz substrates, which can be less highly tolerated without degrading the oscillator stability. However,
SAW oscillators only possess a stability of ~1 part in $10^6$ per deg. C over the required temperature range, hence their medium-term stability is always inferior. Secondly, SAW oscillators are sensitive to instabilities in the phase response of the feedback amplifier. It is for this reason that wideband feedback amplifiers have been predominantly used in SAW oscillator design. However, a low-power tuned loop amplifier with Class C operation is necessary to achieve the improved rf to dc efficiency which is required for battery powered equipment. Thirdly, SAW oscillators current long-term ageing rates (~1 part in $10^6$/month) would necessitate regular equipment realignment. These three deficiencies can be overcome by phase-locking the SAW oscillator to a reference crystal oscillator through a phase-locked loop. Such a module is shown in Fig. 5-1b. This loop when fitted with a summer circuit, to allow direct FM modulation, is able to replace the conventional arrangement shown in Fig. 5-1a. A power amplifier stage is necessary to raise the output to the level required for transmission.
(a) Current radio-telephone transmitter design employing crystal oscillator and a set of multipliers.

(b) New radio-telephone transmitter design based on SAW osc. operating fundamentally at the required frequency.

Fig. 5-1 A comparison between the current design approach to radio-telephones and the new SAW-based module.
5.3 SAW RESONATOR - DESIGN AND PERFORMANCE

5.3.1 Design Parameters

The SAW resonator, whose design is introduced here, was intended to be used as an oscillator frequency stabilising device. For this particular application, the two-port resonator configuration is preferred to the one-port arrangement because of the ease of interconnection [101]. The design parameters, namely: the cavity length, number of reflectors, IDT form and aperture were chosen to satisfy general requirements rather than to achieve the ultimate in performance.

To obtain a high Q, a long cavity and high reflection coefficient are required [51]. A very long cavity, however, gives rise to multi-moding operation. An optimum cavity length of $\sim 130\lambda$ has been suggested [102] for good mode suppression. Also to achieve the resonant condition, the physical cavity length (distance between edges of reflectors) must satisfy the relation $(n + 0.5)\lambda$ [51], where n is an integer.

The transverse mode frequency separation is inversely related to the acoustic aperture. Narrowing the aperture to $(30 - 50)\lambda$ has been found to be sufficient to move the transverse modes off the main peak [102]. But this will result in an increase in the insertion loss, which is undesirable for oscillator applications. Another technique to solve the problem of transverse modes is to apply a cosine overlap weighting to the IDTs in the cavity, this will couple the transducer predominantly to the primary resonant mode $f_o$ [103] and the aperture can then be increased to reduce losses.
The magnitude of the reflection from the reflectors depends on the reflection coefficient of each strip, which is directly proportional to the film thickness \[ h \]

\[ r_e = \frac{1}{3} \cdot \frac{h}{\lambda} \tag{5.1} \]

where

- \( r_e \) = reflection coefficient of single reflection section
- \( h \) = film thickness
- \( \lambda \) = wavelength.

Thick reflectors cause a velocity, hence a frequency, shift \[ h \]. Also they are a source of spurious signals. Convenient designs, therefore, are those with moderate thickness, typically 1500 - 3000 \( \text{Å} \) \[ 51 \], but with a large enough number of reflectors to provide a total reflection coefficient \( r = 0.98 \).

A 2000 \( \text{Å} \) film thickness was chosen. Using Eq. (5.1), the reflection coefficient of each section is then \( r_e = 0.00238 \). Hence for a 2000 \( \text{Å} \) film thickness a minimum number of reflectors of 412 \( \left( \frac{1}{r_e} \right) \) is required.

In a phase-locked oscillator design, a certain amount of resonator tuneability (\( \pm 10 \text{ KHz} \)) is required. This can be achieved by increasing the number of finger pairs in the IDT as is clear from the relation for the resonator bandwidth \[ 51 \]:

\[ \frac{\text{BW}}{f_o} = \frac{L^{1/2}}{\pi L} \frac{|\Gamma| K^2 N}{\pi^2 L} \tag{5.2} \]

where

- \( \text{BW} \) = resonator bandwidth
- \( f_o \) = resonance frequency
- \( \Gamma \) = reflection coefficient
K² = piezoelectric constant
N = number of IDT finger pairs
L = cavity length.

In the light of the above design requirements, the resonator was designed with the following parameters:

- Number of reflectors on each side = 480
- IDT finger pairs = 50
- Cavity length = 107.5 Å
- Acoustic aperture = 150 Å
- Film thickness = 2000 Å.

Although the desired operating frequency was within the UHF band, the experimental resonator was designed to operate at a frequency of 112.7 MHz due to the practical limitation of mask and device fabrication. In principle, this has no effect on the module design philosophy.

The IDTs were placed in the cavity to satisfy the two conditions which are required to ensure maximum coupling of the acoustic energy [51]. These are symmetrical positioning between the two reflectors and location of the centre of the IDT fingers at the peaks of the standing wave.

As the aperture was chosen to be 150 Å to reduce loss, a cosine weighting was applied to the coupling IDTs to avoid the transverse mode problems.

Figs. 5-2 a and b show schematically the resonator design parameters with the predicted standing wave pattern.
5.3.2 Production

The resonator mask was produced on the pattern generator of the Wolfson Microelectronic Liaison Unit of Edinburgh University, in which a pattern can be generated on a photographic plate by flash exposing a series of rectangular images whose dimensions can range from 2 μm to 1010 μm. Any part of a pattern which has a dimension greater than 1010 μm is composed by the abutment of a sufficient number of rectangles. In this resonator design the upper 1010 μm limit causes problems in producing the resonator mask as its aperture was greater than this limit (W = 4.2 mm) and several exposures were required for each strip and finger with a slight amount of overlapping to sustain continuity. The IDT weighting function was accomplished by successive vertical stepping of fingers with control over their lengths to stay within the aperture. This was done because the pattern generator was unable to produce mathematical functions and therefore, the resulting weighting was an approximation to the required cosine function as is clear from Fig. 5-2c, which shows the actual device.

A program, given in Appendix 1, was written on a computer tape to produce the resonator mask on the pattern generator. The mask was then used to manufacture the resonator device.

5.3.3 SAW Resonator Measurements and Results

The two-port SAW resonator produced from the above mask was measured on an HP8410A Network-Analyser. Its frequency response is shown in Fig. 5-3. The insertion loss at resonance was 12 dB and away from resonance was 26 dB.
The loss at resonance was reduced to 5 dB when the resonator was matched to 50Ω system with the aid of an H-P 8414A Polar Display Unit, Fig. 5-4, using series inductors to tune out the IDT static capacitance.

Centre and 3 dB bandwidth frequencies were determined by connecting a C-I 6053 frequency counter to the rf terminal of the network analyser sweep oscillator block, H-P 8553 B, and manually sweeping its frequency. The measured centre frequency was

\[ f_0 = 112.6 \text{ MHz}, \]

which is only 180 KHz different from the theoretical value of 112.78 MHz \( (f_0 = v/\lambda = 3115 \text{ m/s} : 28 \text{ μm}) \). This deviation is believed to be a direct result to velocity dispersion caused by the presence of a large number of relatively thick reflectors \([102]\). However, a 180 KHz reduction in resonant frequency confirms results reported elsewhere \([102/104]\). 3 dB bandwidth \((\Delta f)\) was found to be 45 KHz when the resonator was unmatched and 120 KHz when matched.

The IDT static capacitance \(C_0\) was measured at frequencies away from resonance on an HP 250B R-X meter and was equal to 14.5 PF.

The above measured parameters lead to the determination of the resonator \(Q_s\) (both loaded and unloaded) together with its equivalent circuit elements \((R_1, L_1 \text{ and } C_1, \text{ see Fig. 3-12})\) by the use of the following equations \([50]\)

\[ IL_{\text{resonance}} = -20 \log \left(1 + \frac{R_1}{2R_L}\right) \quad (5.3) \]

\[ = -20 \log \frac{Q_N}{Q_N - 1} \quad (5.4) \]

\[ IL_{\text{resonance}} = -20 \log \left(1 + \frac{R_1}{2R_L}\right) \quad (5.3) \]

\[ = -20 \log \frac{Q_N}{Q_N - 1} \quad (5.4) \]
\[ IL_{\text{away from resonance}} = -20 \log \left(1 + \frac{R_0}{2R_L}\right) \]  
\[ Q_L = \frac{f_0}{\Delta f} \]

where

- \( IL \) = insertion loss
- \( R_L \) = the measuring system load resistor (usually 50Ω)
- \( R_0 \) = the radiation resistance in the shunt model of the IDT alone
- \( Q_N \) = the ratio of unloaded \( Q_u \) to the loaded \( Q_L \) of the device, \( Q_N = \frac{Q_u}{Q_L} \)
- \( \Delta f \) = 3 dB bandwidth.

\( R_1 \) and \( R_0 \) are determined directly from Eqs. \((5.3)\) and \((5.5)\) respectively.

\( Q_N \) determined from Eq. \((5.4)\) is used to find the unloaded \( Q \) of the device \((Q_u = Q_N \cdot Q_L)\) as \( Q_L \) is already known [Eq. \((5.6)\)]. This leads to the determination of \( L_1 \), using Eq. \((3.36)\).

\( C_1 \) can then be found, knowing that at resonance

\[ \omega^2 L_1 = \frac{1}{\omega^2 C_1} \]  

The resonator calculated parameters are given in Table 5-1 and the resonator equivalent circuit is shown in Fig. 5-5, in which theoretical values of \( C_0 \) and \( R_0 \) were calculated by using Eqs. \((3.31)\) and \((3.32)\) respectively.

The resonator insertion loss at resonance was quite adequate for the intended oscillator application, as with such a low loss an oscillator can be constructed with single high gain transistor.
The resonator bandwidth also enables a tuning capability to be achieved to maintain PLL automatic frequency control and FM radio requirements.

SAW resonators are normally judged in terms of their Q and loss at resonance. A comparison in terms of these two factors between the designed resonator and resonators reported elsewhere is given in Table 5.2. It should be noted that these resonators are fabricated with metal strip reflectors. This approach is simple but it gives limited Q values compared to resonators fabricated with grooved reflectors, which are difficult to manufacture but their Q can be close to the material limit [105].

A finger width error of ±0.1 lm (according to Wolfson Pattern Generator data) and film thickness error of 5% due to fabrication can be reasons for weakened coupling and reflection coefficient which are directly related to Q [54]. This may explain the relatively low Q of the 112.6 MHz resonator. Referring to the resonator transmission response in the vicinity of the resonant frequency, Fig. 5-3b, it can be seen that clean single-mode operation has been achieved with the transverse modes effectively removed. This latter property is a very important factor in oscillator design as it eliminates the possibility of frequency instability due to the variations in amplifier gain and circuit phase characteristics.
Fig. 5-2 112.7 MHz two-port SAW resonator intended as a frequency controlling element in an oscillator circuit.

(a) Schematic representation.
(b) Predicted standing wave patterns.
(c) Photo of the actual device.
Fig. 5-3  SAW resonator frequency response:
(a) broad band showing the resonator resonance relative to the IDT sin x/x response and,
(b) around the carrier

Fig. 5-4  SAW resonator transmission response with its both parts tuned to 50Ω resistive load:
(a) losses reduced to 5 dB,
(b) Polar display at matching condition.
Table 5-1 112.7 MHz SAW resonator parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Experiment</th>
<th>Theory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Centre frequency (f_0)</td>
<td>112.6 MHz</td>
<td>112.78 MHz</td>
</tr>
<tr>
<td>Unloaded Q (Q_u)</td>
<td>3.3 x 10^3</td>
<td></td>
</tr>
<tr>
<td>Loaded Q (Q_L)</td>
<td>2.5 x 10^3</td>
<td></td>
</tr>
<tr>
<td>(R_o)</td>
<td>1.895 KΩ</td>
<td>1.85 KΩ</td>
</tr>
<tr>
<td>(R_L)</td>
<td>298 Ω</td>
<td></td>
</tr>
<tr>
<td>(C_1)</td>
<td>0.000056 PF</td>
<td></td>
</tr>
<tr>
<td>(C_o)</td>
<td>14.5 PF</td>
<td>11.3 PF</td>
</tr>
<tr>
<td>(L_1)</td>
<td>1.4 mH</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 5-5 112.7 MHz resonator equivalent circuit
# Table 5-2

A comparison between various SAW resonators manufactured with Aluminium on Quartz both IDTs and reflectors.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>112.6</td>
<td>90</td>
<td>140</td>
<td>393</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Unloaded $Q_u$</th>
<th>焕发</th>
<th>6256</th>
<th>5800</th>
<th>4650</th>
</tr>
</thead>
<tbody>
<tr>
<td>unmatched</td>
<td>2500</td>
<td>4080</td>
<td>4250</td>
<td></td>
</tr>
<tr>
<td>matched</td>
<td>1000</td>
<td>1100</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Loaded $Q_L$</th>
<th>unmatched</th>
<th>12</th>
<th>8</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>matched</td>
<td>5</td>
<td>2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**5.4 SAW RESONATOR STABILISED OSCILLATOR**

SAW resonator stabilised oscillators can be realized with one-port resonators following the conventional approach to crystal controlled oscillators where the one-port device is employed as a substitute for the crystal [104]. However, a degree of difficulty has been experienced with this approach and it has been found that the feedback oscillator technique (see Section 3.2), using a two-port SAW resonator as the feedback network, is easier to design and gives satisfactory results [101]. Here a maintaining amplifier is designed with sufficient gain to overcome the device loss and the two-port resonator is then used to feedback the signal by connecting one of its ports to the amplifier output and the other port to the amplifier input as shown in Fig. 5-6. Following this approach, the resonator device reported in Section 5.3 has been used as a frequency stabilising element in an oscillator circuit.

It was a design aim to build the oscillator with only one transistor stage to reduce power dissipation. Also the maintaining amplifier should have a low noise figure. For these reasons a micro-miniature MMCM 2857 transistor, characterised by its low power dissipation and low noise-figure, was chosen [106]. The transistor provides a gain high enough to overcome the losses in the SAW resonator and the phase-shifting network. The amplifier was designed to be narrow-band using class C operation in order to achieve further gain in terms of rf/dc efficiency.

The amplifier circuit was constructed on a double-sided copper clad board and tested with an input frequency of 112.6 MHz.
The amplifier tank circuit was tuned to give maximum output and minimum unwanted harmonics with the aid of HP 8553B spectrum analyser. The resonator was then fitted to the same board as shown in Fig. 5-7 and interconnected to the amplifier terminals. The circuit returned again. Two 910 nH miniature tuning inductors, connected to the resonator terminals, were required to achieve a proper match to the maintaining amplifier input and output ports. At this stage, the resulting oscillator was tested. It was oscillating at a frequency totally controlled by the SAW resonator, 112.6 MHz, and produced an output power of 12.7 dBm. Its power dissipation was 80 mW with an 11.6 volt supply. This represents an efficiency of 23% at 12.7 dBm rf output.

The SAW resonator-stabilised oscillator circuit diagram is shown in Fig. 5-8. Its output waveform and frequency spectra (both near to and away from carrier) are given in Fig. 5-9, from which the output spectral-purity close to carrier and unwanted harmonics level (-48 dBc) are evident.

To provide frequency tuning, the oscillator circuit was also fitted with a varactor phase shifting network, MV 1401 and R5 (see Fig. 5-8). In response to an external control voltage the varactor changes its capacitance. This will be accompanied with a phase-shift in the oscillator feedback path. This shift is automatically compensated for by a frequency shift so as to maintain the required oscillation condition (2π radians around the loop). For a control voltage ranging from 0 to 10 volts, the oscillator was tuned over 20 KHz with a 14 KHz linear range as shown in Fig. 5-10, in which the slope Δf/Δv represents an oscillator conversion gain of 1.88 x 10⁴ rad/sec/volt.
Fig. 5-6 The basic configuration of a SAW resonator controlled oscillator.

Fig. 5-7 Photo of the 112.7 MHz SAW-resonator controlled oscillator showing both sides of the mounting board.
Fig. 5-8 112.6 MHz SAW resonator-controlled oscillator circuit diagram
Oscillator waveform

Oscillator output spectra around the carrier

Broad-band frequency spectrum showing the fundamental peak relative to harmonics

Fig. 5-9 SAW resonator oscillator output waveform and frequency spectrum.
Fig. 5-10 Frequency versus control voltage characteristic of the SAW resonator stabilized oscillator.
5.5 **PHASE-LOCKED SAMPLER AND LOOP FILTER**

Fig. 5-11 shows a circuit diagram of a sampling phase-detector. This phase detector has been previously used to lock a 460 MHz DL-SAWO intended also for radio-telephone applications [107]. It has a gain constant $K_d = 1$ volt/rad. The detailed circuit operation can be found in reference [108]. The reference frequency, after being amplified and limited, is converted by a step-recovery diode to a train of positive and negative pulses, which are approximately 1.5 volts in amplitude and 0.5 nsec in width. These pulses are then detected and a positive bias is set up on the cathode of CR2 and a negative bias on the anode of CR1. The voltage at the junction of R5 and R6 is nominally zero volts dc.

The rf VCO output is applied to the input of the sampling bridge as shown and is terminated by a 500 ohm load (R1). Diode CR3 detects the rf input at a certain level. The output of the sampling bridge is zero volts when in phase-lock. Any VCO frequency drift will disturb the amplitude balance of the positive and negative pulses at the R5 and R6 junction. An error voltage is then produced with a magnitude proportional to the amount of VCO frequency drift. This error voltage is then applied to the loop filter-amplifier section shown in Fig. 5-12. The loop filter helps to attenuate ac components of the error voltage and provides a certain degree of loop stability (see Section 4.3.1). The output of the filter goes to a high input impedance voltage-follower stage followed by a positive bias circuit, which is required to allow oscillator coarse tuning. A bias voltage of around +4.5 volts was required to centre the oscillator.
frequency within the linear tuning range (see Fig. 5-10). The sampling phase detector output will then change around this bias voltage positively or negatively to pull the oscillator to the correct frequency required to maintain phase-lock. This frequency was exactly equal to ten times the reference, which was supplied from an H-P 8640B locked signal generator.

The loop was provided with an 'integrator + lead' filter (see Table 4-3) to realize type II operation, discussed in Section 4.3.3. The filter elements $R_1$, $R_2$ and $C$ (Fig. 5-12) were calculated according to the design procedure presented in references [77 and 84] for PLLs with active filters.

As FM modulation to the VCO is possible at frequencies beyond the loop bandwidth, the loop cut-off frequency of 300 Hz was necessary to allow speech modulation (frequencies below 300 Hz are greatly attenuated by the voice processor which normally follows the microphone [109]). This leads to the determination of the loop natural frequency, $\omega_n = \text{loop cut-off}/2 = 942 \text{ rad/sec}$.

Referring to Fig. 5-13, which represents the transient response curves for a type II second order viscous damped servomechanism system when disturbed with a step-displacement input [77], selecting an acceptable lock-up curve ($\delta = 0.7$) yields a 5% error with a normalised time $\omega_n t_s = 5$. This is equivalent to a loop settling time $t_s = 5.3 \text{ m sec} (5/\omega_n)$.

Having the values of $\omega_n$ and $\delta$ being determined together with a loop gain $K = K_o K_d = 1.88 \times 10^4$, where $K_o$ and $K_d$ are the gain constants of the oscillator and phase-detector respectively,
then the loop filter elements $R_1$, $R_2$ and $C$ (Fig. 5-12) can be
determined using the design equations [76, 77]:

\[ R_1 C = \frac{0.5 K}{\omega_n^2} \]  \hspace{1cm} (5.8) 

\[ R_2 = \frac{2\delta}{\omega_n C} \]  \hspace{1cm} (5.9) 

From Eq. (5.8), $R_1 C = 10.5 \times 10^{-3}$. A convenient value of
$C = 1 \mu F$ was chosen to give a realizable $R_1 = 10.5 \, K \, \Omega$. With $C$
known, $R_2$ can be calculated using Eq. (5.9), $R_2 = 1.5 \, K \, \Omega$. 
Fig. 5-11 Circuit diagram of the phase sampling detector.

Fig. 5-12 Loop filter inverter, error amplifier and summer.
Fig. 5-13 The PLL phase response to a step position (phase) input for various damping ratios (ref. 77) used in the design of the 112.7 MHz phase-locked SAW resonator module.
5.6 POWER AMPLIFIER

Current radio-telephone equipment requires 100 mW – to 1 W transmitting power. The locked SAW resonator module discussed in the previous section was capable of delivering 19 mW output power. Hence, a power amplification stage was necessary to reach the required transmitting level.

It was decided to reach the required power level with one transistor stage in order to achieve optimum rf/dc efficiency. An RCA 2N4427 transistor was chosen. It is capable of handling input signals of (10 - to 20) mW at VHF frequencies and for such an input range it can develop (300 - to 400) mW carrier output level [110]. Such a capability makes this transistor a convenient device to build the power amplifier stage as its input will be fed from the 19 mW oscillator and its output power will be within the required 100 mW – 1 W level.

The power amplifier design was conventional. P and T matching networks were used and the amplifier circuit was constructed on a double-sided copper clad board as shown in Fig. 5-14a. The power amplifier circuit is shown in Fig. 5-14b.

When the amplifier was tested, it was found to deliver 450 nW from a 19 mW 112.6 MHz input signal with a 12 V supply. It was then connected to the locked resonator-stabilised oscillator and the resulting output was observed on an HP 8553B spectrum analyser. As expected for class C operation, many spurious signals were observed. However, the power amplifier was retuned to minimise these signals and to obtain the maximum possible output level. Fig. 5-14c shows a broad-band spectrum for the power amplifier output. It indicates the unwanted harmonics to be better than -48 dBc.
(a) photo of both sides of the circuit board

(b) circuit diagram

(c) broad-band spectrum indicating carrier level relative to harmonics

Fig. 5-14 The power amplifier
**MODULE PERFORMANCE**

The significance of this new approach to radio-telephone transmitter design can be assessed by comparing the synthesiser performance against commercially available products. A comparison based on component complexity is not valid as the prototype module design has not been optimised. It is suggested that the most relevant assessment of this module is based on a comparison of its power consumption against existing radio-telephone transmitters. The basic SAW oscillator was able to deliver 19 mW output and a class C power amplifier was used to obtain a 450 mW output. The overall module efficiency improves with higher output powers as shown in Fig. 5-15. Efficiencies of 50% can be achieved \([100]\) at 5 W output power. The resonator module efficiency was measured at different output power levels by changing the supply voltage and retuning for maximum signal. Adding the power drain of the sampling phase-detector and reference oscillator gives the projected synthesiser module efficiency shown in Fig. 5-15. This also includes a comparison in terms of rf/dc efficiency between the SAW resonator-based module and existing commercial (FYE pocket-phone) equipment. Also included is the efficiency curve which has been reported in reference \([68]\) for a SAW delay line-based module.

It can be seen that a SAW resonator-based design for portable radio-telephones has significant advantages and deserves serious consideration by equipment manufacturers.
Fig. 5-15 Comparative performance prediction of pocketphone transmitters based on conventional frequency multiplication and SAW phase locked oscillator modules.
6.1 DELAY LINE MEASUREMENTS

This chapter covers the design of two SAW delay line oscillators. These oscillators, intended as a voltage-controlled frequency source in indirect multi-channel synthesizers (Chapter 7), were based on two SAW devices; a 120 MHz SAW delay line designed and fabricated in the Department of Electrical Engineering University of Edinburgh, and a 1480 MHz SAW delay line supplied by Marconi Research Laboratories. They were both subjected to a series of measurements, which were carried out to assess their performance by determining parameters of insertion loss, centre frequency, delay and bandwidth. These measurements and the results obtained are presented below:

i) Impulse Test:

Impulse tests were performed on both delay lines by applying a ~1 nsec 5 volt pulse at 100 KHz pulse-repetition-rate (PRR) from an HP-8004 pulse generator. The output from the delay lines was amplified and displayed on a Tektronix 7904 oscilloscope. Typical traces are shown in Fig. 6-1. The theoretical impulse response is a rectangular RF pulse [19]. The traces show the actual responses have deviations at the pulse ends due to the fact that the input pulse is not ideal. However, the results show good amplitude balance and absence of open circuit IDT electrode fingers.
ii) RF Input Pulse Test:
Tests were also carried out using an input consisting of a 3.2 \mu\text{sec} RF pulse at a centre frequency of 120 MHz for the VHF delay line and \sim 0.1 \mu\text{sec} RF pulse at a frequency of 480 MHz for the UHF delay line. The device responses are shown in Fig. 6-2. The triangular shape results from the convolution of the rectangular input pulse with the rectangular impulse response of the device. Provided that the input pulse is long enough this test can be used to determine the delay line insertion loss at the frequency of the input pulse. The insertion loss is measured by substituting an attenuator for the delay line. The time domain pulsed RF test is also a good method of measuring the delay line frequency response as electromagnetic breakthrough can distort the frequency domain response. The centre and null frequencies of the \sin x/x frequency domain characteristics for both delay lines were measured, on the counter section of the HP 8640B generator which provided the RF signal, at maxima and minima of the time domain traces as shown in Fig. 6-2 (b and c). The measured delay line parameters are given in Table 6-1.

iii) Swept Frequency Test:
The SAW delay line frequency responses were obtained using a HP 8410/2 Network Analyser system. Amplitude and phase characteristics of both delay lines are presented in Fig. 6-3. Centre frequency and 3 dB bandwidth were measured by manual sweeping the frequency of the Analyser's sweep oscillator HP 8690B with a Systron-Donner 6053 frequency counter connected to its RF output. Results are presented in Table 6-2.

The results of these tests could lead to the conclusion
that the available SAW delay lines could be used as stabilising elements in oscillator circuits. Such oscillators should be a single-moded, as predicted from their amplitude and phase characteristics, and would operate with centre frequencies and pull-range capabilities given in Table 6-3.
Fig. 6-1  SAW delay lines impulse responses indicating their amplitude balance and absence of open circuit IDT electrode fingers.

Fig. 6-2  (a and b) SAW delay lines responses to an RF pulse at centre frequency $f_0$. (c) 480 MHz D.L. response to RF pulse at null frequency of the $\sin x/x$ response.
<table>
<thead>
<tr>
<th>DL Parameters</th>
<th>VHF SAW DL</th>
<th>UHF SAW DL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Center frequency $f_0$</td>
<td>119.75 MHz</td>
<td>147.75 MHz</td>
</tr>
<tr>
<td>Insertion loss at $f_0$</td>
<td>34 dB</td>
<td>21 dB</td>
</tr>
<tr>
<td>Delay line length $\tau$</td>
<td>$\sim 2.9 \times 10^{-6}$</td>
<td>$\sim 4.6 \times 10^{-9}$</td>
</tr>
<tr>
<td>Calculated DL length in $\lambda$s $\left[ L = \tau V_s = (\tau f_0)\lambda \right]$</td>
<td>$\sim 348 \lambda$</td>
<td>$\sim 219 \lambda$</td>
</tr>
<tr>
<td>Width of the sin $x/x$ response</td>
<td>700 KHz</td>
<td>4.6 MHz</td>
</tr>
<tr>
<td>Calculated width of sin $x/x$ response $\left( = \frac{2f_0}{L} \right)$</td>
<td>680 KHz</td>
<td>4.8 MHz</td>
</tr>
</tbody>
</table>

Table 6-1 SAW delay line parameters
Fig. 6-3 Amplitude and phase responses of (a) 120 MHz D.L. and (b) 480 MHz D.L.
### Table 6-2 Measured delay lines parameters obtained from swept frequency test.

<table>
<thead>
<tr>
<th>DLs Parameters</th>
<th>VHF DL</th>
<th>UHF DL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Centre frequency $f_0$</td>
<td>119.75 MHz</td>
<td>479.75 MHz</td>
</tr>
<tr>
<td>3 dB bandwidth</td>
<td>$\approx$ 300 KHz</td>
<td>$\approx$ 2 MHz</td>
</tr>
<tr>
<td>Min. insertion loss</td>
<td>35 dB</td>
<td>20 dB</td>
</tr>
</tbody>
</table>

### Table 6-3 Predicted operating parameters of SAW oscillators incorporating the delay lines under test.

<table>
<thead>
<tr>
<th>Oscillator parameters</th>
<th>VHF DL</th>
<th>UHF DL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillation frequency</td>
<td>119.75 MHz</td>
<td>479.75 MHz</td>
</tr>
<tr>
<td>Pull-range ($\pm \frac{f_0}{4L}$)</td>
<td>170 KHz</td>
<td>1.2 MHz</td>
</tr>
</tbody>
</table>
6.2 **120 MHz SAW DELAY LINE OSCILLATOR**

6.2.1 **Oscillator Design and Construction**

This oscillator was designed as a voltage-controlled frequency source (VCO) for a VHF synthesiser loop. Maximum pull-range capability is essential for this purpose to achieve the greatest number of available radio-channels. The oscillator employed the 120 MHz SAW delay line, with the parameters given in Table 6-1, as the feedback element in the oscillator loop (see Chapter 3 for delay line-SAWO theory) with a transistor maintaining amplifier. The amplifier was designed capable of providing a wideband gain of 40 dB. Since the oscillator circuit must have unity loop gain at the operating frequency, a transistor limiter stage was incorporated in the amplifier circuit to act as a non-linear element to reduce the loop gain to unity. The circuit also provided with a buffer stage to minimise loading effects.

The amplifier was constructed on a printed board which also carried the packaged SAW delay line as shown in Fig. 6-4. The detailed circuit is given in Fig. 6-5. Three phase-shifting networks employing MV 1401 and MV 1403 varactors are incorporated in the amplifier circuit as shown. These networks were loaded by other elements in the loop and the required maximum phase-shift (\(\pi\)) was achieved by choosing suitable resistors for the R-C varactor phase-shifters. The amount of phase-shift was observed by recording the oscillator frequency variation with the varactor control voltage delivered from a suitable power supply.
6.2.2 Oscillator Performance

The completed 120 MHz SAW oscillator was tested to determine its capabilities. Its operating frequency, measured with an HP 5245L frequency counter, was controlled by the delay line (120 MHz). The oscillator delivered an output power, measured with an HP 432A power-meter, of 10 mW. The output waveform is shown in Fig. 6-5. The oscillator temperature performance, FM capability and phase-noise were also measured. These later tests are described below and the main oscillator parameters are given in Table 6-4.

i) Temperature Performance: 

The SAW oscillator was located in a 'Montford' environmental chamber with the supply voltage delivered from an external power supply. A digital frequency counter was also connected to the oscillator to measure its frequency. The varactors were replaced by 33 PF capacitors (the varactor mid-range capacitive value) to ensure fixed phase-shift around the oscillator loop and to eliminate the effect of the varactors on the measurements. The chamber temperature was cycled from -10°C to +70°C and the frequency variations of the oscillator were observed on the frequency counter for each temperature step. The overall temperature performance of the oscillator is shown in Fig. 6-6 (curve B) compared against the temperature characteristics (theoretical) of the ST-cut \( \theta = 42.75^\circ \) Quartz substrate of the SAW delay line (curve A) [66]. The parabolic shape of curve B demonstrates that the overall temperature characteristics is governed mainly by the SAW substrate. The discrepancy between curves A and B (Fig. 6-6) is believed to be caused by amplifier non-linearity.
However, the oscillator temperature behaviour is similar to results reported elsewhere. The turn-over temperature occurred at 19°C, which indicates a shift of 2°C from a figure obtained for the delay line substrate alone (21°C). Curve fitting to the oscillator's temperature characteristics gives a second order temperature coefficient of 35 x 10⁻⁹ over a temperature range 0°C to 55°C. This latter figure is very close to that of 32.3 x 10⁻⁹ for the substrate material alone, indicating that the SAW substrate material governs the overall oscillator temperature behaviour.

ii) Frequency Modulation:
A deviation in centre frequency is a direct result of phase changes caused by the amplifier circuit and varactor networks. Capacitor C_T (Fig. 6-5) provides the required frequency trimming and was used to centre the device at 119.95 MHz where maximum output level was observed. Frequency modulation was achieved by varying the varactor control voltage over a range 0 - 10 volts. This resulted in a total frequency deviation (Δf) of ~160 KHz which is equivalent to a phase-shift d = 168° [d (radians) = $\Delta f \times \frac{2\pi L}{f_o}$, where L delay line length in λs]. This frequency deviation was 10 KHz less than the maximum possible (theoretical) pull-range of 170 KHz ($\pm \frac{f_o}{4L}$). Fig. 6-7 shows the oscillator's frequency variation with control voltage, indicating an oscillator conversion gain $K_o = 14 \times 10^4$ rad/sec/volt.

iii) Phase Noise:
The phase noise performance of this oscillator was studied in comparison to an LC-oscillator operating at the same frequency.
to assess the relative merits, in terms of phase-noise, of SAW and LC design approaches to voltage-controlled oscillators. For this purpose, an LC-based VCO was constructed as shown in Fig. 6-8 for operation at 120 MHz. Its operating parameters were:

\[ V_s = 280 \text{ mV} \text{ PK/PK}, \quad C = 40 \text{ pf} \text{ (the mid-range varactor capacitance value)}, \quad L = 44 \text{ nF} \left( \frac{1}{\omega_0^2 C} \right) \text{, and estimated } Q_L \text{ and } Q_C \text{ values of 100.} \]

The SAW delay line oscillator's operating parameters were:

\[ f_0 = 120 \text{ MHz}, \quad Q = 1099 \left( \frac{\pi L_{dL}}{r_{\text{La}}} \right), \quad \text{output power} = 10 \text{ mW, amplifier noise figure of } \sim 3 \text{ dB (estimated) and delay line loss} = 35 \text{ dB.} \]

The theoretical phase-noise performances for the above mentioned oscillators were calculated for different offset frequencies from carrier by substituting their operating parameters in eqs (3.39) and (3.42). Theoretical results are shown in Fig. 6-9. Practical measurements were carried out by phase-locking the oscillators under test to a reference Hewlett-Packard 8640B VHF/UHF signal generator, which was used as a VCO in the measuring system, and mixing to transfer the spectrum to baseband. Measurements were subsequently performed on an HP 8555A Spectrum Analyser following the standard test procedure adopted for the measurement of SSB FM Noise for signal generators [57/112]. The test equipment set-up is shown in Fig. 6-10. The reference oscillator SSB FM Noise is estimated - 135 dB/Hz at 10 KHz offset when operating at 120 MHz [112]. This governs the ultimate sensitivity of this measurement technique. The measured phase-noise characteristics of the oscillators under test are presented in Fig. 6-9, which shows a good agreement between theoretical and measured performance.

The results obtained for both SAW delay line stabilised-
and LC-oscillators indicate that the phase-noise performance for the SAW oscillator with $Q = 10^3$ is superior to the LC oscillator used in this study as would be expected. However, referring to Eqs (3.39) and (3.42) it can be shown that, theoretically, the phase-noise performance of LC and delay stabilised SAWO are comparable when operating at the same output power and $Q$. It is not difficult to design LC and SAW oscillator circuits operating at the same power level at certain frequencies, but a SAWO can operate with a $Q$ much higher than that of the best available LC oscillator circuits. They are thus capable of offering improved signal purity as the oscillator SSB FM Noise is reduced with higher $Q$.

$Q$s of around $10^3$ can only be achieved in LC oscillators by special design [40]. Hence improved phase-noise performance can easily be realized with SAW delay line oscillators having $Q$s exceeding $10^3$. This can be obtained by incorporating a SAW delay line which has a length $L > 300 \lambda$ [Eq. (3.22)], as is the case with the 120 MHz SAWO under consideration.
Fig. 6-4  Photo of the 120 MHz SAW delay line oscillator with the delay line package opened for demonstration.
Fig. 6-5 120 MHz SAW delay line stabilized oscillator circuit diagram.
Table 6-4 Main operating parameters of the 120 MHz SAW delay line stabilised oscillator.
Fig. 6-6 120 MHz SAW oscillator temperature characteristics.

Turn over temperature = 19°C
Temperature coefficient = $35 \times 10^{-9}$
Oscillator conversion gain $K_o = 1.5 \times 10^{-4}$ rad/sec/volt.

Fig. 6-7 120 MHz SAW oscillator frequency deviation versus control voltage.
Fig. 6-8  120 MHz LC - VCO circuit diagram.
SSB FM noise relative to carrier dB/Hz

Fig. 6-9 Phase noise test on 120MHz Oscillator.

(1) ○ - LC VCO
(2) ● - Delay stabilized SAWO 350λ (Q≈10^3)
--- HP8640B Standard used for measurement.
Fig. 6-10  SSB phase-noise test set-up.
6.3 480 MHz DL SAW OSCILLATOR

6.3.1 Oscillator Design and Construction

Two Advantek GPD-401 voltage amplifiers followed by a GPD-402 power amplifier were mounted in series on a 50 \( \mu \) microstrip board to form the maintaining amplifier for the 480 MHz DL-SAWO. The amplifier's characteristics are given in Table 6-5 [113]. They provide enough gain to overcome the 21 dB delay line loss plus expected losses in phase-shifting networks, which are required to control the oscillator operating frequency. The delay line, the parameters of which are given in Table 6-1, packaged in hermetically sealed TO8 capsule was mounted on the same board as the GPD amplifiers as shown in Fig. 6-11. The short transducer of the delay line was connected to the amplifier output and the long transducer to the amplifier input to form the oscillator loop. The oscillator was provided with three R-C phase-shift sections, each consisting of an MV-1401 (or MV 1403) varactor and a resistor. Suitable resistor values were chosen to optimize the oscillator pull-range.

The oscillator circuit configuration is shown in Fig. 6-12.

6.3.2 Oscillator Performance

The 480 MHz delay line SAWO was tested in a similar manner to that of the 120 MHz oscillator (Section 6.2.2) to determine its parameters. The test procedures are not repeated here and only the results are presented and discussed. Table 6-6 gives the oscillator's operating parameters. Its output waveform and spectrum (around the carrier and broadband) are demonstrated in Fig. 6-13, indicating the purity of the output signal at UHF.
frequencies. This is one of the main advantages of these SAW oscillators which results from their ability to provide fundamental operation in such a frequency region.

The temperature performance of this oscillator was determined by measurement carried out with and without the varactors in the circuit. Results were also obtained for different varactor control voltages to study their effect on the oscillator temperature performance. Fig. 6-14 shows a set of curves demonstrating experimental results compared against the temperature characteristics of ST-Quartz ($\theta = 42.75^\circ$). These curves also follow the parabolic temperature behaviour of the delay line substrate material. Non-linearity of the GPD amplifiers believed to be the reason for the discrepancy between the oscillator circuit temperature characteristics (curves B, C and D) and that of the material (curve A). Shifts between curves C and D are due to the frequency deviation obtained with different control voltages applied to the varactor sections. With the varactors present in the circuit the overall characteristics still retain their parabolic shape. However, they show a steeper fall with increasing temperature. Without varactors, the turnover temperature was $17.5^\circ C$ shifted by $3.5^\circ C$ from that of the material. This shift has been further increased to $8^\circ C$ with the varactors present in the circuit (turnover temperature $13^\circ C$).

Curve fitting applied to the oscillator temperature characteristics: (i) with varactors (curve C) gives a second order temperature coefficient of $39 \times 10^{-9}$ over a temperature range ($3 - 20^\circ C$, and (ii) with varactors removed (curve B) gives temperature coefficient $33.9 \times 10^{-9}$. Those figures when
compared to that of the material, $32.3 \times 10^{-9}$, reflect the controlling effect of the temperature characteristics of the SAW material over this range.

The frequency modulation capability of this oscillator was determined by applying a dc control voltage to the varactor phase-shifters. The variation of the output frequency is shown in Fig. 6-15, which demonstrates a nearly linear behaviour over a wide frequency range ($\sim 1$ MHz) and an oscillator conversion gain $K_o (\Delta f / \Delta V) = 10.4 \times 10^5$ rad/sec/volt. The overall frequency deviation obtained for a $(0 - 15)V$ control voltage swing was 1.2 MHz, which is equal to the maximum frequency deviation that can be achieved with this particular oscillator ($\pm f_0 / 4L$, $L = 200\lambda$). Frequency setting can be carried out by the trimming capacitor $C_M$ (Fig. 6-12) which can be used to centre the oscillator at the required frequency.

The phase-noise performance of this oscillator was measured using the set-up described previously. Fig. 6-16 shows the theoretical and measured performance. The theoretical characteristic was calculated by substituting the oscillator parameters; $f_o = 480$ MHz, loss = 21 dB, amplifier noise figure = 3.2, output power $P_o = 7$ mW and $Q = 628$ in Eq. (4.42) and obtain the results for different offset frequencies from the carrier.

Due to the fact that the HP 8640B signal generator, used in the test as a standard frequency source (as shown in Fig. 6-10), has a phase-noise level which is similar to that of the SAWO theoretical curve (see Fig. 6.16), no accurate picture about the SAWO phase-noise performance can be obtained. However, the measured results were found to follow the standard generator
specifications as shown. This means that the phase-noise performance of the standard frequency source has not been degraded by the SAWO under test, which indicates that the phase-noise performance of the SAWO under test is comparable with, if not better than, that of the signal generator used for the test giving $\sim-120$ dB SSB FM Noise level at 10 KHz offset.
Table 6-5 Characteristics of GPD amplifiers used in the design of the 480 MHz oscillator

<table>
<thead>
<tr>
<th></th>
<th>GPD-401</th>
<th>GPD-402</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>13 dB</td>
<td>13 dB</td>
</tr>
<tr>
<td>Gain flatness</td>
<td>± 1 dB</td>
<td>± 1 dB</td>
</tr>
<tr>
<td>Noise figure</td>
<td>4.5 dB</td>
<td>6 dB</td>
</tr>
<tr>
<td>Power output</td>
<td>-2 dBm</td>
<td>+6 dBm</td>
</tr>
<tr>
<td>DC power</td>
<td>+15 V</td>
<td>+15 V</td>
</tr>
</tbody>
</table>

Fig. 6-11 Photograph of the 480 MHz SAW delay line oscillator showing both sides of the mounting board.
Control Voltage (0 - 15V d.c.)

Controlled oscillator

SAW delay line

Fig. 6-12  Circuit connection of the 480 MHz SAW delay line controlled oscillator
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>480 MHz</td>
</tr>
<tr>
<td>Output power</td>
<td>7 mW</td>
</tr>
<tr>
<td>Pull-range</td>
<td>1.2 MHz</td>
</tr>
<tr>
<td>Conversion gain ( K_0 )</td>
<td>( 10.4 \times 10^5 ) rad/sec/volt</td>
</tr>
<tr>
<td>Turnover temperature ( T_0 )</td>
<td>13°C</td>
</tr>
<tr>
<td>SSB FM Noise</td>
<td>-115 dB/Hz at 10 KHz offset</td>
</tr>
</tbody>
</table>

Table 6-6 Main parameters of the 480 MHz SAW delay line oscillator.
Fig. 6-13 The 480 MHz oscillator output waveform and spectrum

(a) Oscillator output frequency waveform
(b) Output spectrum around the carrier BW = 0.3 KHz
(c) Broadband output spectrum
Fig. 6-14 Temperature performance of the 480 MHz SAW delay line stabilized oscillator.
Fig. 6-15 Frequency versus control voltage characteristic of the 480 MHz SAW oscillator.
Fig. 6-15: Phase noise performance of the 480 MHz SAW oscillator.
CHAPTER VII

DESIGN, CONSTRUCTION AND PERFORMANCE OF SAWO-BASED
DIGITALLY CONTROLLED MULTI CHANNEL SYNTHESISERS,
FOR MOBILE RADIO APPLICATIONS

7.1 INTRODUCTION

The advantages of employing SAW oscillators in digital
frequency synthesisers have been highlighted in Chapter 4.

In this chapter the first digital frequency synthesisers
based on SAW oscillators are reported. Since these synthesisers
were intended for Mobile-Radio applications, power dissipation
channel spacing, switching time between operating channels and
FM capability were important design factors. Power dissipation
was minimised through the maximum use of CMOS logic in dividers
design. The synthesisers have also been designed to meet the
requirements for 12.5 KHz channel spacing (recent UK specifi-
cation) [96]. The switching times required depend on the
particular communication system and can range from microseconds
to hundreds of milliseconds [74]. However, an effort has been
made to minimise the synthesiser switching time through optimum
phase-lock designs.

The design, construction and performance of three SAW-
based digital frequency synthesisers are presented:

1. A VHF multi-channel indirect synthesiser, in which a 120
MHz delay line SAWO, reported in Chapter 6, was employed as a
VCO. This synthesiser is capable of generating 12 frequency
channels spaced by 12.5 KHz.
2. A UHF multi-channel indirect synthesiser, where the VCO element was a 480 MHz delay line SAWO, also presented in Chapter 6, with 1.2 MHz pull-range. This synthesiser can generate 96 UHF radio channels at 12.5 KHz spacing.

3. A UHF SAW-based multi-channel 'Gemini' synthesiser, which operates at 480 MHz and is characterised by a fast switching speed capability compared to single-loop indirect synthesis approaches.
7.2 SAW-BASED VHF DIGITAL SYNTHESISER

7.2.1 Synthesiser Design

This synthesiser, shown in block diagram in Fig. 7-1, operates at VHF and follows the indirect design technique. The output from the voltage controlled SAWO is divided and subsequently compared against the reference, crystal controlled, frequency in a phase-comparator. The dc control voltage from the comparator is filtered and fed back to control the SAWO. The loop filter is designed to achieve the required loop bandwidth and provide loop stability. Inserted within the feedback loop is a programmable digital divider, which is programmed from external thumb-wheel switches to provide the multi-channel capability required for communications systems. The module used a 120 MHz SAWO incorporating a readily available 350λ delay line (see Section 6.1). The SAWO, could be tuned from 119.90 MHz to 120.05 MHz, permitting the synthesis of 12 channels with 12.5 KHz spacing.

As in the single channel synthesiser module (Chapter 5), it was desired to minimise the module power dissipation. This dictated the maximum use of CMOS logic. As the highest operating frequency of CMOS is 5 MHz, the output of the SAWO was prescaled in a fixed ECL divider. All other dividers and the phase-comparator of the loop were designed using CMOS logic. This synthesiser is classified as a fixed prescaled PLL system (Section 4.4.2)
7.2.2 The Programmable Divider

A programmable divider is inserted in the synthesiser feedback loop in order to generate multiple stable output frequencies. The programmable division function was achieved with RCA-CD 4059D CMOS synchronous down counter \[14]\), which is a single chip micro-power (30 \(\mu\)W dissipation) device capable of being programmed to divide an input frequency by any number 'N' from 3 to 15,999. Such a division ratio capability can meet the requirement for this particular synthesiser, as its minimum and maximum 'N' values do not exceed the counter limits as shown below:

\[
N_{\text{max}} = \frac{f_{\text{max}}}{f_{\text{ch}}} \quad (7.1)
\]

\[
N_{\text{min}} = \frac{f_{\text{min}}}{f_{\text{ch}}} \quad (7.2)
\]

where

- \(N_{\text{max}}\) = the maximum value of the division ratio in the counter
- \(N_{\text{min}}\) = the minimum value of the division ratio in the counter
- \(f_{\text{max}}\) = the upper limit of VCO pull range
- \(f_{\text{min}}\) = the lower limit of VCO pull range
- \(f_{\text{ch}}\) = channel spacing

The SAWO tuned from 119.90 MHz to 120.05 MHz and the synthesiser operated at 12.5 KHz channel spacing. Hence the programmable counter division ratio ranges from \(N_{\text{min}} = 9592\) to \(N_{\text{max}} = 9604\) (using Eqs. (7.1) and (7.2)).
The output signal from the counter is a pulse, one-clock-pulse wide occurring at a rate equal to the input frequency divided by 'N'. The counter is preset by means of 16 "jam" inputs, as shown in Fig. 7-2, which have been grouped and connected to four BCD thumb-wheel switches. Any required frequency can be selected directly.

The divider is provided with three mode-select inputs, $K_a$, $K_b$ and $K_c$, the logic state of which determines the counters division radix (see Section 4.4.3). The requirement for 12.5 KHz channel spacing, hence a division radix = 8, was achieved by applying the appropriate logic word to the mode-select inputs $(K_a = 0, K_b = 0$ and $K_c = 1)$. This also controls the mode of the last counting section, which is internally connected with the first section, and the overall counter configuration will be as illustrated in Fig. 7-2. The counter can operate at input frequencies up to 5 MHz when supplied with 10 volts.

7.2.3 Fixed Dividers

i) The Prescaler:
As mentioned in Section 7.2.1 this synthesiser is of the fixed prescaled PLL type. The prescaling function was performed with a Plessey SP 8655B low power (50 mW) ECL VHF divider. This fixed counter prescales the 120 MHz SAWO output frequency by a division factor $M = 32$ to a value $f_M$ (3.75 MHz), which can be handled by the following CMOS CD 4059AD programmable divider.

The circuit connection of the prescaler is shown in Fig. 7-3. Its output is CMOS compatible and only a pull-up resistor ($R_1 = 3.3 \, \text{K\Omega}$), connected to the supply line of the CMOS
circuitry, was required to allow the prescaler to drive the variable divider. $R_2$ (3.9 kΩ) is a pull-down resistor, which was connected to the unused input of the prescaler to prevent self-oscillation in the absence of an input signal.

ii) The Fixed Reference Divider:

Phase-comparator input frequencies are normally well below the frequencies of the highly stable crystal controlled oscillators, which are used as reference sources in synthesiser loops. For this reason fixed dividers are employed and the reference is related to the loop comparison frequency by the equation:

$$f_{\text{comp}} = \frac{f_{\text{ref}}}{N_R} \tag{7.3}$$

where

- $f_{\text{comp}}$ = comparison frequency
- $f_{\text{ref}}$ = reference crystal controlled oscillator frequency
- $N_R$ = division ratio of the divider

The comparison frequency in a fixed prescaled PLL is given by:

$$f_{\text{comp}} = \frac{f_{\text{ch}}}{M} \tag{7.4}$$

where

- $f_{\text{ch}}$ = channel spacing
- $M$ = the division ratio of the prescaler in the loop.

Having $f_{\text{ch}} = 12.5$ KHz and $M = 32$, then from Eq. (7.4) the comparison frequency for this synthesiser loop:

$$f_{\text{comp}} = 390.625 \text{ Hz} \tag{7.5}$$
The reference frequency, \(f_{\text{ref}} = 100\ \text{kHz}\), was supplied from a laboratory RCS-102 standard. Knowing \(f_{\text{ref}}\) and the comparison frequency \(f_{\text{comp}}\) (Eq. (7.5)), then the required division ratio of the fixed reference divider can be determined from Eq. (7.3):

\[
N_R = 256 \quad (7.6)
\]

An RCA-CD 4059AD single chip counter (Section 7.2.2) was also chosen to perform the \(N_R\) counting function. This was done by applying a fixed preset code to the BCD "jam" inputs of the counter. This fixed code can be found for any \(N_R\) value. The division ratio, \(R\), for this particular counter is given by:

\[
R = (\text{Mode}) \left[ 10^3 \times \text{decade 5 preset} + 10^2 \times \text{decade 4 preset} + 1 \times \text{decade 2 preset} \right] + \text{Decade 1 preset} \quad (7.7)
\]

Mode 10 was chosen. This leads directly to the basic counter configuration shown in Fig. 7-4a, from which (using Eq. (7.7)):

\[
N_R = 10 \left[ 10 \times 2 + 1 \times 5 \right] + 6 = 256 \quad (7.8)
\]

The fixed code, to the "jam" inputs, which corresponds to the chosen counter mode and to the required division ratio is given in Fig. 7-4b.

7.2.4 Phase-Comparator, Loop Filter and Error Amplifier

i) Phase-Comparator:

The phase-comparator employed in this synthesiser loop was a type II PD, which forms a section of the RCA-CD 4046A CMOS PLL.
This phase-detector was chosen because it possesses many features which make it attractive for frequency synthesis. Detailed technical information is given in Reference (114) and only its important features are mentioned here. It is an edge-controlled digital memory network consisting of four flip-flops and control gating which turns a p- or n-type FET ON or OFF as schematically illustrated in Fig. 7-5a. If the reference frequency $f_{\text{ref}}$ is higher than the loop signal frequency ($f_{\text{MN}}$; see Fig. 7-1), the p-type output driver is maintained ON continuously. If the signal input frequency is lower than the reference frequency, the n-type output driver is maintained ON continuously. When the reference and signal frequencies are the same, but the reference input lags the signal input in phase, the n-type output driver is maintained ON for a time corresponding to the phase-difference. When the input frequencies are the same, but the signal input lags the reference in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. The output of this PD effectively consists of current pulses, which when applied to the loop filter produced a voltage which is automatically adjusted until the reference and signal inputs are equal in both phase and frequency. At this stable point, both p- and n-type output drivers remain OFF and thus the phase-comparator output becomes an open circuit and holds the voltage at the output of the filter constant. In normal circumstances, the low-pass filter will lose charge, even through high impedance paths. In order to maintain the desired dc level, a small error pulse is generated from the phase comparator, momentarily turning the p-channel transistor
ON to compensate for the lost charge [73].

The phase-comparator circuit is also capable of producing a 'phase-pulse' output at a high voltage level, which can be used for indicating a locked condition. For this purpose a light-emitting diode has been employed as shown in Fig. 7-5b. Typical waveforms of this phase-detector are given in Fig. 7-6 [114].

It should be noted that this phase-comparator acts only on the positive edges of the input signals and is therefore not sensitive to duty cycle.

ii) Loop filter:

It was intended to use a type 2 PLL. The advantages of such an approach have been discussed in Section 4.3.3. To achieve this the loop filter has to meet two requirements. Firstly, it must provide an integration function, so that two integrators will be incorporated in the loop, the VCO and the filter. Secondly, it must be able to produce a voltage output from a current input supplied by the phase-detector discussed above. Such a filter has been described by Thrower, Allen and Atkinson [82/85] and is shown in Table 4-3. It has a transfer function given by:

\[ \frac{V_o}{I_i} = \frac{1}{C_1} \frac{1 + sT_e}{s(1 + sT_a)} \]  (7.9)

where

\[ T_e = R_1(C_1 + C_2) \]  (7.10)

\[ T_a = R_1C_2 \]  (7.11)

Type 2 loops incorporating current type phase-detector
and lag-lead integrator filter have been analysed in references (82) and (85), where a design procedure has been produced to determine the filter elements \( C_1, C_2 \) and \( R_1 \) for optimum loop performance. This design procedure has been followed in the design of the synthesiser under consideration, as described below:

Initially a suitable value of loop natural frequency \( \omega_n \) is chosen, so that a certain loop bandwidth can be achieved. Due to the presence of the fixed prescaler, the comparison frequency was limited to 390.625 Hz (see Section 7.2.3). This puts a limitation on the loop bandwidth and hence on the natural frequency. \( 120 \) Hz \((753.9 \text{ rad/sec})\) bandwidth was selected to achieve a reasonable operating point, hence \( \omega_n = 251 \text{ rad/sec} \) as for such loops

\[
\omega_{3dB} = 3 \omega_n \quad \text{(7.12)}
\]

A useful design should employ \( \omega_n \) within a range \((2 \times 10^2 - 1 \times 10^3)\) rad/sec. Hence the chosen \( \omega_n \) was within this range.

Having

\[
\omega_n = \frac{1}{\sqrt{T_e T_a}} \quad \text{(7.13)}
\]

where \( T_e \) and \( T_a \) are defined in Eq. (7.10) and (7.11) respectively.

Then

\[
\frac{1}{\sqrt{T_e T_a}} = 251 \quad \text{(7.14)}
\]

A design factor \( R \) can now be calculated using the following equation:

\[
R = \frac{\sqrt{T_e T_a}}{T_s} \quad \text{(7.15)}
\]
where
\[ T_s \text{ (sampling period)} = \frac{1}{f_{\text{comp}}} \]

\( f_{\text{comp}} \) is given in Eq. (7.4).

Using Eqs. (7.5), (7.14) and (7.15), then \( R = 1.56 \).

Using the frequency v.s. voltage characteristics of the SAW oscillator (Fig. 6-7), employed as a VCO in the system, the maximum and minimum conversion gains (\( K_o = \frac{d\Phi_o}{dV_c} \)) are \( 1.4 \times 10^4 \) and \( 0.47 \times 10^4 \) respectively. Thus the oscillator gain ratio is:
\[
G_R = \frac{K_o \text{ max}}{K_o \text{ min}} = 2.97
\]

Referring to the design chart shown in Fig. 7-7, for \( R = 1.56 \) and a gain ratio \( G_R = 2.97 \) gives \( T_e/T_a = 17 \) and \( K_m = 0.21 \).

Knowing \( K_m \) leads directly to the determination of \( \frac{I_o}{C_1} \) using the equation:
\[
K_m = \frac{T_s^2 \cdot I_o}{C_1 \cdot N_{\text{min}}} \left( \frac{d\Phi_o}{dV_c} \right)_{\text{max}}
\]

where
\[
T_s = \text{ sampling period } ( = \frac{1}{f_{\text{comp}}})
\]
\( I_o \) = phase-detector output current
\( N_{\text{min}} \) = minimum division ratio of the programmable divider
\( ( = 9592) \)

Then:
\[
\frac{I_o}{C_1} = 13.84 \times 10^3
\]

The phase-comparator employed can deliver a driving current
up to 2.5 mA. Hence, using Eq. (7.18), suitable values for $C_1$ and $I_0$ are: 0.14 μF and 2 mA respectively.

Having $T_e/T_a = 17$ and using Eq. (7.14), then:

$$T_e = 16.32 \times 10^{-3}$$  \hspace{1cm} \text{(7.19)}

and

$$T_a = 0.96 \times 10^{-3}$$  \hspace{1cm} \text{(7.20)}

Using Eqs. (7.10) and (7.11) with $C_1$ known, the other filter components can now be determined: $R_1 = 109.7$ KΩ and $C_2 = 8.75 \times 10^{-9}$ F. Practically the chosen filter components were: $R_1 = 100$ KΩ, $C_1 = 0.15$ μF and $C_2 = 10$ nF as shown in Fig. 7-8.

The time constant $T_e$ is related to the loop settling time $t_s$, $t_s = 2 T_e$. Hence theoretically, the expected switching time for this particular loop is 32.64 m sec.

iii) Error Amplifier:

In order to cover the full SAWO deviation range, the control voltage must swing from 3 to 12 volts. As the maximum output voltage from the phase-detector/filter combination is 10 volts, an error amplifier was employed to achieve a dc amplification of 1.2. This error amplifier was also designed to provide a dc offset voltage equal to 3 volts, so that when the phase-detector voltage is at its lowest level (0 volt) the amplifier output is 3 volts. This offset voltage was required for proper SAWO operation (see Fig. 6-8). The error amplifier circuit diagram is shown in Fig. 7-9. The first stage is an adder circuit, where the input control voltage is added to the zener-diode.
voltage. The second stage is an inverter amplifier providing 1.2 dc amplification.

7.2.5 Synthesiser Performance

The VHF synthesiser module, shown in Fig. 7-10, used a 120 MHz SAW oscillator incorporating a 350A SAW delay line. The long delay (∼3 μ sec) restricted the number of available channels in this experimental synthesiser to 12. The prescaling by 32 reduced the comparison frequency by the same factor from 12.5 KHz to 390.625 Hz. This restricted both the loop gain and tuning time. Before adopting the integrator filter, reported in Section 7.2.4, several filters were employed and the loop performance in terms of switching speed was studied. The lag-lead integrator filter (Fig. 7-8) gave the best results.

The loop performance was determined by measuring its settling time. This was done by comparing the synthesiser output frequency against a reference generator operating at the same frequency as shown in Fig. 7-11. The experiment began with the synthesiser under test and the reference generator, operating in a locked condition, running at output frequencies differing from each other by a channel spacing (say 119.925 and 119.9375 respectively). These output frequencies are compared in a mixer, the output of which is connected to an oscilloscope through a LPF. The output of this filter is the difference frequency. Synthesiser is then switched to a frequency equal exactly to that of the reference (119.9375). The output of the filter becomes dc after a transition period, which is a measure of the loop settling time, as shown in Fig. 7-12. The measured time was 50 m sec.
This figure approximates the theoretical estimation (around $2T_\text{e} = 32.64 \text{ m sec}$) for this particular loop which is comparable to that achieved with practical VHF avionic synthesisers [72]. However, when observing the loop control line (the dc voltage to the VCO), it was noticed that the comparison frequency component (390.625 Hz) was not well attenuated by the filter. As such a component is a source of residual FM noise on the VCO output [78], a single-pole R-C filter was added to the loop. This resulted in a clean dc control voltage, but the switching time increased considerably (up to $\sim 150 \text{ m sec}$). This increase in switching time was expected due to the further reduction in loop bandwidth which resulted from the added filter. This degraded performance has resulted in a more sophisticated approach in the design of the UHF synthesisers described in the following sections.

The main VHF synthesiser module parameters are presented in Table 7-1.
Fig. 7-1  SAW-based VHF digital frequency synthesiser
Fig. 7-2 Connection to the BCD switches and mode inputs of the Prog. counter.

Fig. 7-3 The prescaler \((M = \pm 32)\) circuit
Fig. 7-4  Counting sections configuration (a) and digital code (b) required to achieve 256 division ratio in the fixed reference divider, CD 14059

Fig. 7-5  (a) Phase-comparator connection
(b) Lock-indicator circuit
Fig. 7-6  Phase comparator waveforms:
(a) reference leads the signal input,
(b) equal phase and frequency,
(c) reference lags the signal input.

Fig. 7-7  Loop optimization design chart (ref. 82).
from Phase-comparator to error amp.

\[ C_1 = 0.15 \mu \text{f} \]
\[ C_2 = 10 \text{ n}\text{f} \]
\[ R_1 = 100 \text{ K}\Omega \]

Fig. 7-8 Loop filter

\[ \kappa_3 = - (\kappa_1 + \kappa_2) \]
\[ \frac{\kappa_4}{\kappa_3} = - \frac{R_3}{R_2} = 1.25 \]

Fig. 7-9 Error amplifier designed to provide 1.6 d.c. amplification and +3 volts offset.
Fig. 7-10 Photograph of the complete VHF synthesiser module
Fig. 7-11 Experimental set-up for measurement of the synthesiser tuning time.
Fig. 1-12 Switching time measurement of the VHF synthesiser

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>120 MHz</td>
</tr>
<tr>
<td>Number of channels</td>
<td>12</td>
</tr>
<tr>
<td>Channel spacing</td>
<td>12.5 KHz</td>
</tr>
<tr>
<td>Type of prescaling</td>
<td>fixed</td>
</tr>
<tr>
<td>Switching speed</td>
<td>50 - 150 m sec</td>
</tr>
<tr>
<td>Power consumption</td>
<td>~ 90 mW</td>
</tr>
</tbody>
</table>

Table 7-1 VHF synthesiser parameters
7.3 SAW BASED UHF DIGITAL SYNTHESISER

7.3.1 Synthesiser Design

In a multi-channel frequency synthesiser which retains a low loop cut-off frequency to permit direct modulation of the SAWO with the voice input, there is a limit to the minimum oscillator Q. The Q must be sufficiently high to maintain a narrow oscillator line width stopping the transmitter radiating excessive energy [(-90) dBc] into adjacent radio channels. This sets a minimum Q value of \( \sim 500 \) at \( f_o = 1480 \) MHz (a typical UHF operating frequency). Equation (3.22) subsequently yields the minimum delay line length as \( L = 160\lambda \). The 1480 MHz SAWO described in Section 6.3 was designed with 200\( \lambda \) delay line and therefore is suitable for UHF synthesis where high adjacent channel suppression and large numbers of radio channels are desirable. For this reason, this oscillator was employed as the VCO element in the UHF synthesiser loop reported here.

The design approach to this UHF synthesiser avoided the restricted comparison frequency which resulted when a fixed pre-scaler is inserted before the variable divider by incorporating a dual modulus prescaling technique (Section 4.6.2). This approach allows improved performance with little added complexity and a moderate power consumption (mainly consumed in the ECL prescaler). The complete system is presented in block diagram in Fig. 7-13. The programmable dividers, phase-detector and reference fixed divider were designed with CMOS to reduce the overall power-dissipation.
7.3.2 Dual-Modulus Prescaler and Buffer Amplifier

The dual modulus prescaling technique is covered in Section 4.6.2. The circuit of the prescaler which has been employed in the UHF synthesiser loop is shown in Fig. 7-14. It consists of two stages. The first stage, an SP 8685, is a two-modulus (10/11) high speed counter. Its division ratio is controlled by two inputs, FE1 and PE2, such that it will divide by 10 when either input is in the high state and by 11 when both inputs are at the low state. PE2 was connected to zero level while PE1 to the control circuit. The second stage, the control circuit, is a divide by '8' SP 8794 counter designed for use with dual modulus prescalers. Its division radix (8) has been chosen to satisfy the requirement for 12.5 kHz channel spacing [Eq. (4.26)]. Moreover, it increases the division ratio of the prescaler while retaining the same difference in division ratio. Thus a divide by 10/11 becomes a divide by 80/81. Hence it can bring the output frequency of the whole prescaler into the region where CMOS or low power TTL can be employed. The control circuit is provided with a control input through which the division ratio (80/81) can be controlled by counter B (Fig. 7-13).

The prescaler's first stage is capable of accommodating input frequencies up to 500 MHz. However, in the second stage, the control circuit, internal delays do not permit operation at frequencies above 40 MHz. If the SAWO is connected directly to the prescaler the input to the control circuit will be 48 MHz (480/10) and it will not function. For this reason a divide by 2 ECL stage was necessary before the prescaler combination to bring the frequency within the operating range. This divide by
2 function was performed with a low power SP 8607 high speed divider. Its circuit is shown in Fig. 7-15.

The use of a fixed divide by 2 stage reduces the loop comparison frequency from 12.5 KHz to 6.25 KHz (Eq. (7.4)). However, such a comparison frequency is still fairly high and gives more freedom in the loop design than the 390,625 Hz obtained with the VHF fixed prescaled synthesiser (Section 7.2).

The input circuitry of the UHF prescaler presents a non-linear impedance. Since the prescaler is driven by a voltage controlled oscillator which is also intended to provide a spectrally pure signal, it was necessary to isolate the VCO from the divider input so that the SAW-VCO output is not degraded. An Avantek GPD-401 [95] amplifier was employed to provide the necessary isolation (up to 20 dB). This also provided a signal gain of 13 dB.

7.3.3 Programmable Divider

The output frequency of the prescaler combination was 3 MHz (480/2 x 80). Such a frequency can be handled by CMOS logic which was chosen for the design of the programmable divider circuit in order to minimise the loop power consumption.

As can be seen from Fig. 7-16, the programmable divider consists of two sections: the 'B' counter and the 'N' counter. The total division ratio \( N_T \) achieved by this combination (in series with the dual-modulus prescaler) is given in Eq. (4.20) and the required division range can be calculated from:
\[ N_T \text{ max} = \frac{f_{o \text{ max}}}{f_{\text{ch}}} = \frac{480.5 \times 10^6}{12.5 \times 10^3} = 38440 \]  
(7.21)

\[ N_T \text{ min} = \frac{f_{o \text{ min}}}{f_{\text{ch}}} = \frac{479.3 \times 10^6}{12.5 \times 10^3} = 38344 \]  
(7.22)

where

\[ f_{o \text{ max}} \] = the maximum output frequency of the UHF SAW oscillator

\[ f_{o \text{ min}} \] = the minimum output frequency of SAWO

\[ f_{\text{ch}} \] = channel spacing

With the prescaler modulus of 80/81, the minimum division ratio of the programmable divider below which the system will not function is 6400 (calculated using Eq. (4.24) with \( P = 80 \)). From Eq. (7.22) the required minimum division ratio is 38344 which is much higher than the critical 6400 figure. Hence the system is not limited in that regard.

The divider sections 'B' and 'N' are described below:

i) The 'B' counter:

Referring to Eq. (4.21), for the programmable divider to operate correctly the 'B' counter division ratio must be within the prescaler's base modulus (80). Consequently, it must be programmed between '0' and '79'. Furthermore, the 'B' counter must consist of two stages; a radix '8' first stage for programming 12.5 KHz steps (see Section 4.43) followed by a decade stage to achieve the maximum count (80). The counter was constructed with two cascaded 4 bit, HD-74C163 CMOS binary counters connected and programmed as shown in Fig. 7-16a.
ii) The 'N' counter:
The 'N' counter must be programmed from 479 to 480 (the overall
division ratios of the divider divided by counter 'B' radix).
Hence three decade stages are required. The counter was formed
in the conventional way from 3 HD-74C 162 CMOS decade counters
[115] as shown in Fig. 7-16b.

7.3.4 Reference Divider

The incorporation of a fixed divide by '2' prescaling stage
in the synthesiser loop reduces the comparison frequency to 6.25
KHz [calculated using Eq. (7.4) with \( f_{ch} = 12.5 \) KHz and \( M = 2 \)].
The reference frequency was 100 KHz, supplied from a laboratory
RCS-102 standard. Hence to achieve a reference input to the
phase-comparator equal to 6.25 KHz \( (= f_{comp}) \) a division ratio of
'16' [Eq. (7.3) with \( f_{ref} = 100 \) KHz and \( f_{ch} = 12.5 \) KHz] was
required. This division function has been achieved with two
stages ('1:8' followed by '1:2') of CD 4017A CMOS fixed dividers
as shown in Fig. 7-17. The quad 2 input NOR, CD 4001A, is
required for proper divider operation. The output, 6.25 KHz, was
connected to the reference input of the phase-comparator.

7.3.5 Phase-Comparator, Loop Filter and Error Amplifier

Due to its advantages, the type 2 phase-comparator, part
of a CD 4046A, Fig. 7-5, described in Section 7.2.4 was also
employed in the design of the UHF single loop synthesiser. The
reference and signal inputs of the comparator were connected to
the outputs of the reference divider and the programmable divider
respectively. The loop comparison frequency was 6.25 KHz
A lag-lead integrator filter was also employed to realize a type 2 PLL. The filter components, \( C_1, C_2 \) and \( R_1 \), were determined according to the design procedure described in Section 7.2.14 with the following loop parameters:

i) Loop natural frequency, \( \omega_n = 628 \), chosen in order to achieve 300 Hz bandwidth allowing FM modulation with the audio signal from a voice processor.

ii) Sampling period \( T_s = 1.6 \times 10^{-4} \ (1/f_{\text{comp}}) \).

iii) Minimum division ratio of the programmable divider \( N_{\text{min}} = 38344 \).

iv) Maximum and minimum conversion gains of the 480 MHz SAWO equal to \( 16.5 \times 10^4 \) and \( 7 \times 10^4 \) respectively, obtained from Fig. 6-15.

The loop filter is shown in Fig. 7-18. The time constant \( T_e \), to which the loop settling time is related was \( 3 \times 10^{-3} \). Hence the expected switching time for this synthesiser is within the range \( (3 - 6) \) m sec (see Section 7.2.5).

The SAW oscillator control voltage must swing from 0 to +16 volts to achieve its maximum pull-range (1.2 MHz). The output from the phase comparator-filter combination is less than 10 volts. Hence an error amplifier is required. A single 741 op-amp circuit with a non-inverting dc gain of 1.7 was designed to perform this function as shown in Fig. 7-18.

### 7.3.6 UHF Synthesiser Performance

The SAW-based UHF synthesiser module is shown in Fig. 7-19. It covers the \((479.3 \text{ to } 480.5)\) MHz frequency band allowing the
synthesis of 96 radio channels spaced at 12.5 KHz. The main synthesiser parameters are presented in Table. 7-2. Phase-lock was achieved throughout the full 1.2 MHz SAWO pull-range with reference and signal inputs to the phase-comparator equal in both frequency and phase as shown in Fig. 7-20. The switching time was measured using the method described in Section 7.2.5. Fig. 7-21 shows the loop response for a 100 KHz frequency step observed on the control (dc control to SAWO) and phase lines (see Fig. 7-11). These traces indicate ~4 m sec switching time, which is within the expected (3 - 6) m sec range for this particular loop (see Section 7.3.5). The comparison frequency component can be seen clearly from Fig. 7-21a within the 4 m sec transition period. Beyond this period, when the loop has settled to its new control voltage level, the control line is a clean dc voltage. This indicates that the loop filter is capable of attenuating the comparison frequency components. No further filtering was therefore required. This is a direct result of the increased 'comparison frequency' allowed by the dual-modulus design approach.

With the summer circuit shown in Fig. 7-22a, incorporated in the loop, the synthesiser FM capability was investigated. The audio frequency was varied from 0.3 KHz to 20 KHz. During this test, the loop kept in lock as it is evident from Fig. 7-22b which also shows the response of the loop to a 100 KHz frequency step, measured on the loop control line, with the modulating frequency (2 KHz) super-imposed on the controlling dc signal.
Fig. 7-13
Block diagram of UHF SAW-based frequency synthesiser.

- Reference
  100 KHz

- CMOS 
  Loop tutor

- 480 MHz DL-SAWC

- \( f_{\text{ref}} \)

- CMOS
  P.D.

- Digital switches

- Loop filter
  Error Amp.

- CMOS
  M.N

- CMOS
  counter

- CMOS
  N

- CMOS
  counter

- CMOS
  B

- CMOS
  \( \div 16 \)

- CMOS
  \( \div 2 \cdot 2 \cdot 1 \)

- ECL
  \( \div 80/61 \)

- ECL
  \( \div 50 \)

- ECL

- Buffer

- \( f_0 \)

- \( f_{\text{out}} \)

- \( f_0 = 480 \) MHz

- \( f_{\text{out}} = 480 \) MHz

- \( \text{BW} = 1.2 \) MHz

- \( \text{ch} = 12.5 \) KHz
Fig. 7-14 Circuit connection of the \( \div 80/81 \) dual modulus prescaler.

Fig. 7-15 Circuit connection of the \( \div 2 \) high speed divider.
Clock input from the prescaler
To the control input of the dual-modulus prescaler
'Signal input' To Phase-Comparator

Fig. 7-16 Programmable divider circuit diagram. (a) 'B' counter and (b) 'N' counter.
Fig. 7-17 UHF synthesiser reference divider.

From P.D. to SAWO

\[ C_1 = 0.01 \mu F \]
\[ C_2 = 0.05 \mu F \]
\[ R_1 = 250 \, K\Omega \]
\[ R_2 = 1.3 \, K\Omega \]
\[ R_3 = 1.8 \, K\Omega \]

Fig. 7-18 Loop filter and error amplifier.
Fig. 7-19 Complete UHF digital frequency synthesiser incorporating 480 MHz DL-SAWO

<table>
<thead>
<tr>
<th>Operating frequency</th>
<th>480 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>96</td>
</tr>
<tr>
<td>Channel spacing</td>
<td>12.5 KHz</td>
</tr>
<tr>
<td>Type of prescaling</td>
<td>dual modulus</td>
</tr>
<tr>
<td>Switching time</td>
<td>4 m sec</td>
</tr>
<tr>
<td>Power consumption</td>
<td>220 mW</td>
</tr>
</tbody>
</table>

Table 7-2 UHF synthesiser parameters
Fig. 7-20  Input frequencies to the phase-detector in the UHF loop, showing equal phase and frequency.

\[ \Delta V_C = 100\text{KHz} \]

\[ t_s = \text{switching period} \]

Fig. 7-21  Switching time measurement of the UHF synthesiser showing phase (a) and d.c. control (b) responses.
Fig. 7-22 (a) Adder/inverter circuit used to modulate the UHF loop with audio signal.

(b) Loop response to 100 KHz frequency step with modulating signal \( f_m \) applied to the loop.
7.4 SAW-BASED UHF 'GEMINI' SYNTHESISER

7.4.1 System's Design and Construction

Gemini synthesisers, discussed in Section 4.5, represent the simplest approach to indirect synthesis loops in which the channel spacing does not put an upper limit on the loop comparison frequency, as the case with single loop synthesisers. This allows loop designs with very large bandwidth leading to improvements in synthesiser 'switching speed' and 'phase-noise' performance. The achievable improvement in phase-noise, however, depends on the reference oscillator frequency and noise floor as well as the loop bandwidth.

The main objective of this design was to realize a fast-switching synthesiser (1 m sec switching time) operating at UHF incorporating SAWO. To achieve this, it was decided to develop the 480 MHz single loop synthesiser, reported in Section 7.3, into a Gemini system as shown in the block diagram of Fig. 7-23. The following additional components were required:

i) Dual-modulus prescaler and a programmable divider;
ii) mixer;
iii) band-pass filter; and
iv) another stable oscillator to deliver the interpolating frequency \( f_1 \).

The additional dual-modulus prescaler and programmable divider were designed and constructed in a similar manner to the dividers given in Sections 7.3.2 and 7.3.3. The mixing was achieved with SN 76514 IC mixer, and an NE 565 IC-PLL was employed to perform the bandpass filtering function as described in
Since the division ratios of the programmable dividers 'N' must be equal, the dividers were connected in parallel with their counting modes programmed from the same frequency selection switches as shown. In the locked condition, the input frequencies to the phase-comparator are equal.

Hence:

\[
\frac{f_o}{2N_T} = \frac{f_1}{N_T} + f_R
\]

(7.23)

where

- \(f_o\) = output frequency
- \(f_1\) = interpolating input frequency
- \(N_T\) = total division ratio of the programmable dividers
- \(f_R\) = reference input frequency

From Eq. (7.23) the output frequency \(f_o\) for this particular system is given by:

\[
f_o = 2f_1 + N_T(2f_R)
\]

(7.24)

It is clear from Eq. (7.24) that the maximum channel spacing achieved with this system is:

\[
f_{ch} = 2f_R
\]

(7.25)

Hence, for 12.5 KHz channel spacing, \(f_R\) is equal to 6.25 KHz. This frequency was supplied to the system from RCS-102, 100 KHz reference divided by '16' using the CMOS fixed reference divider shown in Fig. 7-17.

Referring to Fig. 7-24, which demonstrates the predicted
phase-noise for this system, to achieve optimum phase-noise performance the loop bandwidth should not exceed the indicated limit (line A). Hence, a 120 MHz comparison frequency has been chosen in order to obtain a loop bandwidth around the optimum value. Also this figure gives reasonable bandpass filter characteristics. Once the comparison frequency is determined, the interpolating frequency $f_1$ can be found as described below:

\[
\text{Having, } f_{\text{comp}} = \frac{f_0}{2N_T}
\]

Then, at VCO mid-range frequency, $f_0 = 480$ MHz.

$N_T$ is given by:

\[
N_0 = 2000
\]

Knowing $f_{\text{comp}}$, $f_R$ and $N_T$, the interpolating frequency $f_1$ can be obtained from Eqs (7.23):

\[
f_1 = 227.5 \text{ MHz}
\]

This frequency, $f_1$, was supplied from HP 8640N locked generator. The requirement for a high frequency oscillator with a stability as good as the reference $f_R$, makes the Gemini system practically difficult to design. However, by using a SAW oscillator this problem can be solved as suggested in Chapter 8, keeping the requirement for only one crystal reference as it is the case with single loop synthesisers.

The completed Gemini system is demonstrated in block diagram in Fig. 7-25. The loop filter was redesigned in accordance with the new loop parameters, namely: $f_{\text{comp}} = 120$ KHz and $N_{\min} = 1952$ (see Section 7.4.2). This resulted in the following loop filter components, $R_1 = 500$ K\Omega, $C_1 = 0.4$ nF and $C_2 = 42$ pF.
7.4.2 Bandpass Filter and Mixer

Referring to Fig. 7-23, the bandpass filter must be able to discriminate between the wanted frequency \(\frac{f_1}{N_T} + f_R\) and the unwanted products from the mixer: \(\frac{f_1}{N_T} - f_R\), \(\frac{f_1}{N_T} + 2f_R\) and higher order harmonics. This means that if the filter pass-band is to be centred on the wanted frequency it must be able to reject the frequencies, \(\frac{f_1}{N_{T\min}}\) and \(\frac{f_1}{N_{T\max}} + 2f_R\). The system operating range covers 96 channels, hence the total variation in the programmable counter division ratio '\(N_T\)' is:

\[\Delta N = 96\]

Having:

\[N_{T\min} = N_0 - \frac{\Delta N}{2}\] (7.26)

and

\[N_{T\max} = N_0 + \frac{\Delta N}{2}\] (7.27)

where

\[N_0 = \text{the division ratio of the programmable counter at mid-range frequency},\]

and knowing \(N = 2000\) and \(\Delta N = 96\), therefore \(N_{\min} = 1952\) and \(N_{\max} = 2048\). Hence the nearest unwanted frequencies are:

\[\frac{f_1}{N_{T\min}} = 116.54\ \text{KHz} \quad \text{and} \quad \frac{f_1}{N_{T\max}} + 2f_R = 123.58\ \text{KHz}\]

Another factor to consider is that \(f_1/N\) will vary as \(N\) is varied to change the output frequency. Thus unless the filter is to be tunable the percentage passband must be greater than the percentage variation in \(N\), in other words:

\[B_{\text{pass}} = \frac{\Delta N}{N} \times 100\%\] (7.28)
For $N = 2000$ and $N = 96$, $B_{\text{pass}} = 4.8\%$. This is equivalent to 5.76 KHz. The amount of ripple that can be tolerated within the passband and the out of band rejection necessary are dependent on the type of logic used in the phase-comparator. As the phase-comparator used CMOS logic, 3 dB of passband ripple would be acceptable and 11 dB of out of band rejection would be necessary.

Fig. 7-26 shows the worst case characteristics required for this filter. It had been intended to use an R-C active filter but the offset rejection requirements and the frequency involved made such approach unsuitable and it was decided to use a phase-locked loop as a filter. The PLL can act as a filter by locking on to any signal within the capture range which must be equal to the passband and rejecting all signals outside this range. There would be an output signal from such a filter whether or not there was any input signal in the desired frequency range but this does not matter in this case since there will always be a signal in this frequency range. An integrated-circuit PLL, NE 565 which gives a CMOS compatible square wave output when operated from ±10V supplies was used to perform the filtering function. One of the advantages of using a PLL as a bandpass filter in this application is that the input to the filter can be of varying magnitude and waveshape and yet the output is of constant amplitude and waveshape, suitable for driving the CMOS phase-comparator in use, thus it acts as a combined filter and signal conditioner. A block diagram of the NE 565 and the external components necessary to use it as a bandpass filter is shown in Fig. 7-27.

The free running frequency of the VCO is given by:
\[ f_V = \frac{1.2}{4R_1C_1} \text{ Hz} \quad (7.29) \]

\( R_1 \) should lie between 2 and 20 kΩ. Setting \( R_1 \) equal to 5 kΩ, the value of \( C_1 \) to give a free running frequency of 120 KHz is 500 pF.

The lock-range of the device is given by:

\[ f_L = \pm \frac{8f_V}{V_{cc}} \text{ Hz} \quad (7.30) \]

\( V_{cc} \) was 10 volts to make it compatible with CMOS power supply.

This gives:

\[ f_L = \pm \frac{8 \times 120}{10} = \pm 96 \text{ KHz} \]

This was reduced to \( \pm 0.2 f_V \) by shorting pins 6 and 7 and setting the gain control resistance to zero. This gives a lock-range of:

\[ f_L = \pm 19.2 \text{ KHz} \]

The capture range, \( f_c \), using a simple low-pass filter is given by:

\[ f_c = \frac{1}{2\pi} \left( \frac{2\pi f_L}{\tau} \right)^{\frac{1}{2}} \quad (7.31) \]

where

\[ \tau = 3.6 \times 10^3 \times C_2 \quad (7.32) \]

The required capture range is \( \pm 2.9 \text{ KHz} \) (3 dB bandwidth of the filter). Using a lock-range of \( \pm 19.2 \text{ KHz} \) in Eq. (7.31) gives:

\[ \tau = 3.63 \times 10^{-4} \]

Hence, using Eq. (7.32):

\[ C_2 = 0.1 \mu\text{F} \]
The filter was tested alone before inserting it in the system. Its output was found to follow the input frequencies as long as they were located within the capture range. Outside this range, the output frequency returns to its free running value $f_v$ (unlock condition), which was adjusted by changing the values of $R_1$ or $C_1$ (Eq. (7.29)) until exactly 120 KHz was obtained.

The mixing function in the Gemini loop was performed by a Texas Instruments 8N 76514 double-balanced mixer. Due to the fact that the input signals to the mixer were square waves, one of which $\frac{f_1}{2N_T}$ had a very small mark to space ratio, the original mixer circuit was modified; firstly by the use of a monostable multivibrator, SN 74121, to stretch the narrow pulse input to obtain a mark to space ratio of about 1 to 1, and secondly by the addition of simple R-C filters at the inputs of the mixer. These modifications help to reduce the unwanted harmonics down to the (-80)dB level and the nearest unwanted signal, the carrier, to 50 dB less than the sum and difference signals. The complete mixer circuit is shown in Fig. 7-28.

7.14.3 Gemini Loop Performance

The Gemini loop operated at 480 MHz permitting the synthesis of 12.5 KHz spaced channels over the full SAWO pull-range (1.2 MHz). However, it was noticed that at the pull-range extremes, the output frequency reverted to its mid-range value (480 MHz). This meant that the passband of the NE 565-PLL filter (see Section 7.14.2) was not large enough to accommodate the full frequency swing. Attempts to extend this band were made by changing the value of $C_2$ (Fig. 7-27), but it was found difficult to
precisely achieve the required 5.76 KHz.

The loop switching time was measured using the set-up shown in Fig. 7-11. Traces 'a' and 'b' of Fig. 7-29 demonstrate the loop response to 100 KHz frequency step, from which it is evident that the loop was able to operate with a switching time less than 1 m sec (\(\approx 700 \mu\text{sec}\)). This figure is within the projected value.

Fig. 7-29a shows a rippled dc control voltage to the VCO. The feedthrough due to long unshielded wiring is believed to be the cause of this effect.

The spectra of the synthesiser output, both broad-band and close to carrier, are shown in Fig. 7-30. When trace 'b' is compared to that of the oscillator alone (Fig. 6-13b) it can be seen that the contaminated dc control voltage has degraded the oscillator purity. Carefully shielded wiring together with an improved bandpass filter design should result in a Gemini loop with satisfactory performance.
Fig. 7-23 Block diagram of 480 MHz Gemini Synthesiser.
Fig. 7-24 Predicted phase noise characteristics of the 480 MHz 'Gemini' system.
Fig. 7-25 Detailed block diagram of the 480MHz Gemini Synthesiser.
Fig. 7-26 Bandpass filter requirement (worse case characteristics).

Fig. 7-27 Circuit diagram of the PLL B.P.F.
Fig. 7-28 Mixer circuit diagram.
Fig. 7-29 'Switching time' measurements of the Gemini system.
(a) Control voltage and (b) Phase-comparison output.

Fig. 7-30 Output spectra of the Gemini synthesiser.
(a) Broad band and (b) Close to the carrier.
7.5 SUMMARY

The design and performance of three SAW-based multi-channel digital frequency synthesisers have been covered in the previous sections. All of them follow the indirect technique of frequency synthesis. A comparison between their overall characteristics is given in Table 7-3.

The use of a high Q SAWO limited the number of available radio channels in the VHF synthesiser to 12. By contrast the lower Q SAWO operating at UHF allowed the synthesis of 96 radio channels in the UHF synthesiser.

The relatively long switching time obtained with the VHF loop was a direct result of the incorporation of a '32' fixed prescaler. This was overcome in the design of the UHF loops, where dual-modulus prescaling systems were used. A ¼ m sec switching time was obtained with the single loop UHF synthesiser.

The third synthesiser, designed using the Gemini configuration, provided the same operating characteristics as the UHF single-loop system, but with a faster switching speed. However, a number of additional components, eg. mixer and bandpass filter, were required together with the need for a RF stable oscillator to produce the interpolating frequency.
Parameters | VHF Synthesiser | UHF Synthesiser | Gemini
---|---|---|---
Operating frequency | 120 MHz | 480 MHz | 480 MHz
Number of channels | 12 | 96 | 64
Channel spacing | 12.5 KHz | 12.5 KHz | 12.5 KHz
Type of prescaling | fixed | dual-modulus | dual-modulus
Switching speed | 50 - 150 msec | 4 msec | 0.7 msec
Power consumption* | 90 mW | 220 mW | 480 mW

* not including the VCOs

Table 7-3 Comparison between the SAW synthesisers reported in Chapter 7
CHAPTER VIII

CONCLUSION

The research described in this thesis was carried out to assess the potential applications of Surface Acoustic Wave Oscillators in personal radio-telephones and in multi-channel communications systems.

The high Q, high fundamental frequency and low insertion loss of SAW resonators allows the design of oscillators with improved phase-noise performance and rf/dc efficiency. Such features are a major attraction in personal radio-telephones. However, the direct incorporation of a SAWO is currently not possible as the medium and long term stabilities (temperature performance and ageing rate) of SAWOs are not compatible with the stability requirement of these equipments. A phase-locking technique was therefore used to control the SAWO from a reference bulk crystal oscillator to overcome this limitation. A SAWO resonator-based single-channel radio-telephone module has been designed and constructed. In this module, a 2:1 improvement in rf/dc efficiency, compared to existing radio-telephone equipment, was achieved. The module also demonstrated a clean output signal.

Certain applications require personal radio-telephones with more than one channel. Commercial equipment utilise several crystals to provide the multi-channel operation. The SAW module can, however, provide this type of operation by the incorporation of several SAW resonator devices, operating directly at the required frequency, which can be switched to a common wideband maintaining amplifier. This configuration has the advantage of providing several operating channels with the requirement for only one bulk crystal oscillator (acting as a
reference for the phase-locked loop) instead of many. This would make the device more compact and rugged, although the overall efficiency will be degraded due to the presence of the untuned common amplifier.

In comparison with existing personal radio-telephones SAW resonator modules offer improved ruggedness, immunity to mechanical vibration and signal purity. Their use therefore deserves serious consideration by equipment manufacturers.

The LC-oscillators, currently employed in communication synthesisers as frequency sources, are relatively unstable and their 'phase-noise' characteristics are normally poor due to the practical difficulty of achieving good Q values. Their noise performance limits the number of channels that can be used in a given frequency band because of adjacent channel interference. Since the number of users in the VHF/UHF band is presently increasing very rapidly, a closer channel spacing (hence improved phase-noise) is therefore required to match this increase. With phase-noise becoming an important factor, SAW oscillators could be very useful. SAW delay line controlled oscillators can be designed with a pull-range which enables them to cover hundreds of radio channels. Unlike LC-oscillators, their Q can be made sufficiently high to give satisfactory phase-noise performance. This has been demonstrated by two DL-SAWOs designed to operate at VHF and UHF frequencies. Both oscillators were successfully employed as frequency sources in phase-locked indirect synthesisers, which were able to provide multi-channel operation in response to a digital command.

Communication synthesisers normally operate in two modes, transmit and receive. This type of operation requires controlled oscillators with a pull-range wide enough to cover the frequency bands required
for both modes allowing for the intermediate frequency separation between them. This whole frequency band can normally be covered by a single LC-oscillator which, in this aspect, is superior to the DL-SAWO as the pull-range of the latter is limited to a maximum frequency shift of $\sim 1\%$. However, this limitation in the DL-SAWO pull-range can be overcome in practice by the employment of two SAW delay lines, operating at centre frequencies separated by the IF, which can be switched to a common amplifier from the $T_x/R_x$ switch which also controls the programmable divider of the synthesiser. Alternatively, multi-mode SAW oscillators such as that described in reference (90) could be used for this purpose when designed with two frequency modes separated by the required IF. This added complexity might be justified in future communication systems which operate with very close channels and require high adjacent channel suppression, a feature which is difficult to achieve with LC-oscillators particularly at higher operating frequencies ($> 500$ MHz).

Recently, frequency hopped mobile-radio systems operating at UHF have been proposed. This requires synthesiser designs with a fast switching speed capability ($< 1$ m sec) and low noise frequency sources. Here, SAW oscillators can also be useful. This was demonstrated in a UHF SAW based synthesis system designed and constructed in a 'Gemini' phase-locked loop configuration. The drawbacks of this system are its relatively complex circuitry and the requirement for a highly stable RF reference input. However, the RF input could be supplied from a SAW resonator operating at the required frequency. This resonator oscillator could be locked to the same crystal oscillator which is used as a reference source.

The future applications of SAWO in practical systems depends on
commercial as well as technical factors. They have already proved valuable as frequency sources in radar [32]. They could also be very useful in communications, but their ageing rate needs to be improved and a considerable amount of work is presently being carried out in this area. In the phase-locked communication synthesisers described in this thesis, the ageing problem was overcome by employing a stable reference. These synthesisers will become more attractive as international regulations move towards closer channel spacing.

One of the major advantages of SAW oscillators is their high fundamental frequency. The upper limit to this is limited by the practical requirement for IDT finger resolution. This fabrication problem can now be reduced by using devices based on the surface skimming bulk wave (SSBW) mode of operation where a higher fundamental frequency can be obtained for the same finger resolution [116]. Also since SSBW are not confined to the substrate surface an improved ageing rate may result. Oscillators based on surface skimming bulk wave and their applications are important research topics for future work.
REFERENCES


20 C S Hartmann, D T Bell, Jr, R C Rosenfeld, "Impulse model design of acoustic surface wave filters", IEEE Transactions, MTT-21, 4, April 1973.
The impact of new technologies in signal processing, IEE Conference Publication No. 144, 1976

32a) R E Stigall, "SAW devices for use in a high performance television tuner".


48 P M Grant, A D Milne and D P Morgan, "Private communications".


57 "Understanding and measuring phase-noise in the frequency domain", Hewlett-Packard Application Note 207, October 1976.

58 P Sample and B Callaway, "4601 180 MHz frequency synthesiser", Solartron-Schlumberger Technical Note, 1975.


62 P C Duckett, R J Peduto and G V Chizak, "Temperature compensated crystal oscillators".


79 "Phase-locked loops", Signetics Applications Note on Digital, Linear and MOS ICs", pp 6/1-6/8, 1974


85 K Thrower, "Private communications".

86 R E Funk, "Low-power digital frequency synthesisers utilising COS/MOS ICs", RCA Application Note ICAN-6716, 1975.


W J Tanski and H Van der Vaart, "The design of SAW resonators on Quartz with emphasis on two-port", Ultrasonics Symposium, 76 CH120-5SU, pp 260-265, 1976.


P.M. Grant, "Private communication".


113 "Design with GPD amplifiers", Avantek Application Notes.


APPENDIX I

PROGRAMME FOR THE 112.7 MHZ SAW-RESONATOR MASK
APPENDIX I

Programme for the 112.7 MHz SAW-Resonator Mask

/*R.MUSSAI. 13.6.1977
WEIGHTED IDS TWO PORTS RESONATOR

F1
INT
AA
AT
DE 0
IT
140 0
AT
ED
DE 1
IT
260 400
AT
ED
DE 2
IT
260 -400
AT
ED
S 70 6410
-90000 -20000
INT
CK 0 475
O 6400
CN 0 479
0 16400
CH 0 475
O 25200
CK 0 479
O 33550
CI 0 479
97230 C
CM 0 475
97230 6400
CK 0 479
97230 16400
CK 0 479
97230 25200
CM 0 479
97230 33550
CM 0 479
S 70 7350
67305 10000
CM 1 25
67305 17320
CM 1.25
67305 24650
C1 1 25
74445 0
CM 1 24 74445 7320
CM 1 24 74445 14650
CM 1 24 74585 19600
CM 2 24 74585 26920
CM 2 24 74585 34250
CM 2 24 67445 9800
CM 2 24 67445 17120
CM 2 24 67445 24450
CM 2 24 67445 34520
CM 2 24 83125 9600
CM 2 24 83125 17120
CM 2 24 83125 24450
CM 2 24 83125 34520
CM 2 24 83125 46250
CM 2 24 74305 -2020
CM 2 24 74305 5320
CM 2 25 74305 12650
| CM | 2 25 | 74445 21980 |
| CM | 1 24 | 74445 29320 |
| CM | 2 24 | 74445 36650 |
| CM | 1 24 | 82985 -12020 |
| CM | 1 24 | 82985 -4680 |
| CM | 2 24 | 82985 2650 |
| CM | 1 24 | 89985 -2020 |
| CM | 2 25 | 89985 -5320 |
| CM | 2 25 | 89985 12650 |
| CM | 2 25 | 83125 31580 |
| CM | 2 24 | 83125 36920 |
| CM | 2 24 | 83125 46250 |
| CM | 2 24 | 90125 21980 |
| CM | 1 24 | 90125 29320 |
| CM | 1 24 | 90125 36650 |
| CM | 1 24 | S 7200 6020 |
| CM | 1 24 | 67280 -8000 |
| CM | 1 24 | 74200 -8000 |
| CM | 1 24 | 82980 -8000 |
| CM | 1 24 | 89680 -8000 |
| CM | 1 24 | 67280 43980 |
| CM | 1 24 | 74200 43980 |
| CM | 1 24 | 82980 43980 |
| CM | 1 24 | 89680 43980 |
APPENDIX II

A LETTER AND A PUBLICATION

RELATED TO THE AUTHOR'S WORK
Professor J.H. Collins, BSc, MSc, CEng, FIEEE, FIEE,
Department of Electrical Engineering,
University of Edinburgh,
King's Building,
Mayfield Road,
Edinburgh,
EH9 3JL

Dear Professor Collins,

It gives me great pleasure to convey to you the Council's decision to award you, Mr P.M. Grant, Mr R.C. Corner and Mr K.M. Hussain the A.F. Bulgin Premium for your joint paper on 'Mobile radio frequency synthesizers based on surface acoustic wave oscillators'. This paper was considered to be the outstanding contribution published in the Institution's Journal during 1977 on components and circuits. The value of the award is £25, to be shared between you.

Premiums may be taken in the form of books or scientific instruments, and I would be glad to know as soon as possible the form in which you would like to take your award. Please let me have the fullest possible details (e.g. titles, publishers etc... of books) so that arrangements to comply with your wishes may be put in hand without delay.

The presentation of the Institution's premiums traditionally takes place at the Annual General Meeting, which this year will be held in London on Thursday, 5th October, at 6 p.m. in the Goldsmiths' Theatre at the London School of Hygiene and Tropical Medicine, Keppel Street, Gower Street, London, WC1. I hope you will be able to attend to receive your award in person, and perhaps you will let me know nearer the date whether you will be able to do so.

May I conclude by offering you my warmest congratulations on this well-deserved award.

Yours sincerely,

F.W. Sharp
Editor
Mobile radio frequency synthesizers based on surface acoustic wave oscillators


SUMMARY
Delay-stabilized surface acoustic wave oscillators are attractive for use as stable, low-noise sources in digital frequency synthesizers for mobile radio. Here the design and operating principles of the surface acoustic wave oscillator are briefly reviewed. Its application is subsequently detailed in three experimental frequency synthesizer modules, which phase lock the surface acoustic wave oscillator to a reference crystal oscillator to achieve the superior stabilization required in mobile radio applications. First a single channel u.h.f. synthesizer is described which replaces the frequency multipliers in existing u.h.f. radiotelephone transmitters with a S.a.W.O. operating directly at 460 MHz carrier frequency. The requirement for accurate long and medium-term frequency stability, ±6 parts in 10^6 is met by controlling the saw oscillator directly from a stable hulk crystal oscillator with a phase locked loop. The module maintains lock over the −10°C to +40°C temperature range with a ± 10% adjustment of the supply voltage. By careful choice of loop time constants, the s.a.w.o. can also be frequency modulated. Thus, the module can be used to retrofit v.h.f./u.h.f. personal radiotelephones. The module is later extended, with variable divider logic, into multichannel frequency synthesizers, e.g. Fig. 2. Preliminary results are presented for both v.h.f. and u.h.f. s.a.w.o.-based synthesizers. Alternative designs of synthesizers incorporating s.a.w.o.s are included and their relative advantages discussed. The experimental modules reported here were designed primarily to demonstrate operating principles, and hence were not optimized either in terms of efficiency or power output.

1 Introduction
The delay stabilized surface wave oscillator (s.a.w.o.) 1-4 possesses several features which could prove attractive for mobile radio applications. When compared with conventional crystal oscillators (based on bulk acoustic wave resonators) the advantages of s.a.w.o.s are rugged construction, high fundamental operating frequency (10 MHz-2 GHz), output powers up to 1 W, and low single sideband (s.s.b.) f.m. noise performance. A significant attraction is the ability during design to trade off the oscillator Q to give either high stability (Q ~ 10000) or a frequency deviation capability up to 1% of the operating frequency (Q ~ 100). This latter feature ultimately permits a single s.a.w.o. to cover several v.h.f./ u.h.f. radio channels. Therefore, the s.a.w.o. characteristics are intermediate between the bulk crystal oscillator and LC voltage-controlled oscillator (v.c.o.). (See Table I.) However, s.a.w.o.s do not possess either the ultimate long-term stability of the former or the electronically-controllable octave bandwidth of the latter. For completeness the resonator stabilized s.a.w.o. 5 has been included in Table 1. However, its restricted deviation precludes its use in multichannel synthesizers and hence it is not considered further in this paper.

Delay-stabilized s.a.w.o.s have many potential uses in communication, radar and telemetry equipments. This paper describes the design and operation of three experimental mobile radio frequency synthesizer modules incorporating these s.a.w.o.s. First a single channel synthesizer (Fig. 1) is reported which replaces the frequency multipliers in existing u.h.f. radiotelephone transmitters with a s.a.w.o. operating directly at 460 MHz carrier frequency. The requirement for accurate long and medium-term frequency stability, ±6 parts in 10^6, is met by controlling the s.a.w. oscillator directly from a stable bulk crystal oscillator with a phase locked loop. The module maintains lock over the −10°C to +40°C temperature range with a ± 10% adjustment of the supply voltage. By careful choice of loop time constants, the s.a.w.o. can also be frequency modulated. Thus, the module can be used to retrofit v.h.f./u.h.f. personal radiotelephones. The module is later extended, with variable divider logic, into multichannel frequency synthesizers, e.g. Fig. 2. Preliminary results are presented for both v.h.f. and u.h.f. s.a.w.o.-based synthesizers. Alternative designs of synthesizers incorporating s.a.w.o.s are included and their relative advantages discussed. The experimental modules reported here were designed primarily to demonstrate operating principles, and hence were not optimized either in terms of efficiency or power output.

2 S.A.W. Oscillator Principles
The delay stabilized s.a.w.o., shown schematically in Fig. 1, comprises a delay line whose output is amplified and fed back to the input. S.a.w.o. delay lines (Fig. 3) are fabricated on polished quartz substrates by depositing
Table 1. Comparison of properties of various oscillators.

<table>
<thead>
<tr>
<th>Oscillator type</th>
<th>Operating mode</th>
<th>Frequency range (Hz)</th>
<th>Effective loaded $Q$</th>
<th>Deviation</th>
<th>Temperature coefficient</th>
<th>S.s.b. f.m. noise at 10 kHz offset from 500 MHz source</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional quartz crystal</td>
<td>resonator stabilized</td>
<td>$10^4-2 \times 10^7$</td>
<td>$5 \times 10^3-2 \times 10^6$</td>
<td>up to 500 parts in $10^6$</td>
<td>$&lt; 1$</td>
<td>$-140$ (multiplied 10 MHz)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LC-based voltage controlled</td>
<td>resonator stabilized</td>
<td>$10^5-10^6$</td>
<td>$10^4-10^5$</td>
<td>up to octave bandwidth</td>
<td>typically 10</td>
<td>$-100$</td>
</tr>
<tr>
<td>Surface acoustic wave</td>
<td>resonator stabilized</td>
<td>$10^6-2 \times 10^9$</td>
<td>$10^5-10^6$</td>
<td>$&lt; 100$ parts in $10^6$</td>
<td>$\sim 1$</td>
<td>no measured results</td>
</tr>
<tr>
<td>delay stabilized</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$10^2-10^4$</td>
<td>$10^4-10^5$ parts in $10^6$</td>
<td>$-105$ to $-140$ (Q dependent)</td>
<td></td>
</tr>
</tbody>
</table>

and subsequently etching a 500–2000 Å aluminium film to yield the desired interdigital transducer (i.d.t.) patterns. The s.a.w. velocity of 3157 m/s introduces a delay of $\sim 3 \mu s/c m$, resulting in a wavelength, $\lambda$, of 6·8 µm (i.d.t. finger width 1·7 µm) at 460 MHz. When the amplifier gain exceeds the delay line loss oscillation occurs according to the phase condition:

$$\phi_n + \frac{2\pi f_n L}{v} = 2\pi n$$

where $L$ is the acoustic path length, $f_n$ the frequency of the $n$th mode, $v$ the acoustic velocity and $\phi_n$ the phase shift through the feedback loop. This oscillator multimodes at a comb of frequencies spaced by $1/T_0$, where $T_0$ is the loop transit delay, which is approximately $L/v$. However, the s.a.w. delay line is a frequency filter whose response is controlled by the i.d.t. geometries. Oscillator delay lines are usually designed with a (sin $x$)/$x$ frequency response where the main lobe peak coincides with the desired operating frequency, $f_o$. When the nulls are arranged to suppress the unwanted frequencies stable (single mode) operation is achieved.

This oscillator can now be deviated by altering the feedback delay with an electronically controlled phase shifter. Selection of a $\pm \pi/2$ phase shift provides a frequency deviation,

$$\Delta f = \pm \frac{f_o}{4L}$$

without upsetting the single-mode operation. Thus, the selection of $L$ which controls directly the oscillator $Q$ (Ref. 3)

$$Q = \pi L$$

and hence the spectral linewidth and s.s.b. f.m. noise performance also sets the available deviation. Analysis

---

Fig. 1. Single channel synthesizer module.
MOBILE RADIO FREQUENCY SYNTHESIZERS BASED ON SURFACE ACOUSTIC WAVE OSCILLATORS

is currently aimed at establishing the maximum modulation rate for s.a.w.o.s. Modulation indices of unity have been achieved in s.a.w.o.s employing modulation rates of $10^6$ Hz. Measurements of short-term stability on high-power, 5 W, s.a.w.o.s have shown results which are comparable with, if not superior to, existing crystal oscillator performance (Table 1).

Several problems hinder the direct incorporation of s.a.w.o.s in radiotelephones. First, the oscillator medium-term (temperature) stability must meet the $\pm 3$ kHz u.h.f. radiotelephone requirements over the $-10^\circ$C to $+40^\circ$C operating temperature range. This can be achieved with crystal oscillators based on AT cut bulk acoustic wave resonators possessing a crystal cut angle tolerance of $\pm 1'$ of arc. The most stable s.a.w.o.s are fabricated on ST cut quartz substrates, which can be less highly tolerated without degrading the oscillator stability. However s.a.w.o.s only possess a stability of $\sim 1$ part in $10^6$ per deg C over the required temperature range, hence their medium-term stability is always inferior. Secondly, the s.a.w.o. is sensitive to instabilities in the phase response of the feedback amplifier. It is for this reason that wideband feedback amplifiers have been predominantly used in s.a.w.o.s. Here we have explored the feasibility of incorporating a low-power tuned loop amplifier with a class C power amplifier to achieve the superior d.c. to r.f. efficiency which is required for battery powered equipments. Thirdly, s.a.w.o. current long-term ageing rates ($\sim 1$ part in $10^6$/month) necessitate regular equipment realignment. These three deficiencies have been overcome in the following synthesizer modules by phase locking the s.a.w.o. to a reference crystal oscillator. Although the ultimate deviation of a s.a.w.o. (1%) is small compared to a v.c.o., s.a.w.o. based synthesizers are well matched to the bandwidth of existing u.h.f. pre-tuned radiotelephone equipments.

3 Single-channel Frequency Synthesizer

3.1 460 MHz S.A.W. Oscillator

The 460 MHz $L = 400 \lambda$ delay line, which was fabricated on a 7.6 mm x 1.8 mm (0.3 in x 0.7 in) rhombic shaped ST, X quartz substrate (Fig. 3(b)), was characterized by exciting it with a shortburst of r.f. signal. The insertion loss was 21.5 dB at the centre frequency of 459-73 MHz and the delay was 870 ns. The s.a.w.o. was constructed with a narrowband feedback amplifier, comprising three tuned MMT 2857 transistor stages, with 30 dB open loop gain. Output power of 0.2 mW was obtained for 64 mW d.c. input. Both the efficiency and output power level can be improved with class C tuned power amplifiers. The electronically variable phase shift was obtained with a CR network. Variation of the BA 141 varactor diode reverse bias between 1 volt and 7 volt altered its capacitance from 17 pF to 4 pF giving a 50° change in the phase shift through the network. This deviated the oscillator by 160 kHz. When temperature cycled from $-10^\circ$C to $+40^\circ$C the u.h.f. output from the

![Fig. 2. V.h.f. s.a.w.o.-based synthesizer](image)

![Fig. 3. S.a.w. delay line](image)

May 1977
s.a.w.o. altered by 30 kHz. This temperature performance can be improved by almost an order of magnitude when a wideband feedback amplifier is used. However, in principle this oscillator possesses sufficient electronically-controllable frequency adjustment to compensate for all temperature effects, power supply tolerances ageing mechanisms, and permit f.m. deviation of 5 kHz to be achieved.

3.2 Phase-locked Sampler

The sampling phase detector used a step recovery diode to convert the reference input from the crystal oscillator into a train of short (500 ps) pulses. These pulses drove a diode bridge which sampled the s.a.w.o. output and subsequently held it in a f.e.t. buffer amplifier. When combined with the 460 MHz s.a.w.o. the open-loop gain was approximately $10^5$ s$^{-1}$. The phase detector power consumption was 400 mW. Our s.a.w.o. synthesizer was designed for a low-pass loop with a low audio cut off frequency, 40 Hz. This permits the loop to track slow transients, e.g. temperature and ageing effects, without responding to the oscillator modulation. In addition the $-6$ dB/octave audio pre-emphasis severely attenuates any s.a.w.o. deviation at modulation rates below 100 Hz.

3.3 Synthesizer Performance

The 460 MHz synthesizer module was constructed with a 10 MHz laboratory standard supply supplying the reference frequency. Figure 4(a) shows a spectrum analysis of the s.a.w.o. module output with no modulation input. In comparison Fig. 4(b) shows the output when deviated 5 kHz by the 1 kHz audio tone shown in the upper trace of Fig. 5. The lower trace of Fig. 5 shows the demodulated 460 MHz output. The similarity between traces of Fig. 5 gives no evidence of any distortion from the phase control loop. Phase lock was maintained, with no change in the output frequency, while the module was temperature cycled from $-10^\circ$C to $+40^\circ$C and the power supply adjusted $\pm 10\%$.

The significance of this new approach to u.h.f. radiotelephone transmitter design can be assessed by comparing the synthesizer performance against commercially available products. A comparison based on component complexity is not valid as the prototype module design has not been optimized. With the recent launch of commercially available s.a.w. i.f. filters for domestic colour television receivers, which cost only 90p in quantity production, it is our opinion that any doubts as to the reliability and availability of s.a.w. delay lines should now be unfounded. Contrary to the television requirement the s.a.w.o. has a much higher tolerance of delay line fabrication errors as the precise filter characteristic is not a prime factor in maintaining stable oscillation.

It is suggested that the most relevant assessment of our module is based on a comparison of its power consumption against existing radiotelephone transmitters. Although the basic s.a.w.o. is inefficient, when the feed-
back amplifier is operated at low loop power (1–10 mW),
to minimize d.c. power consumption, and class C
amplifiers are employed to obtain the required (100
mW–1 W) output, then the overall oscillator efficiency
will improve with higher output powers as shown in
Fig. 6. Efficiencies of 50% have already been achieved
at 5 W output power. Adding the power drain of the
sampling phase detector and reference crystal oscillator
gives the projected synthesizer module efficiency shown
in Fig. 6. When compared against existing UK Pye
Pocketphone equipments the efficiency of our module
should be comparable with these equipments up to ∼ 100
mW output power. Above this level we predict that the
s.a.w.o. based design of u.h.f. transmitters has significant
advantages, hence it now deserves further serious con-
sideration by equipment manufacturers. These single
channel synthesizers, employing narrow oscillator devia-
tion, can in principle be implemented with either delay or
resonator stabilized s.a.w.o.s. The lower insertion loss of
the s.a.w. resonator is a major attraction in battery
powered equipments.

4 Multichannel Frequency Synthesizers

4.1 V.h.f. Synthesizer Design

Our first demonstration multichannel synthesizer,
which operated at v.h.f. (Fig. 2), followed standard
indirect design techniques where the output from the
voltage controlled s.a.w.o. is divided and subsequently
compared against a reference crystal controlled frequency
in a phase comparator. If the variable divider is pro-
grammed to count in unity increments then the com-
parison frequency equals the channel spacing, 125 kHz.
The d.c. control voltage from the comparator is filtered
and fed back to control the s.a.w.o. The loop filter can
again be designed with a cut-off at low audio frequencies
permitting direct modulation of the s.a.w.o. with the
voice or data input.

As in the earlier module the prime goal is to minimize
the power consumption. This dictates that maximum use
must be made of complementary metal oxide silicon
(c.m.o.s.) logic. Unfortunately, the maximum operating
frequency of c.m.o.s. is 5 MHz, hence the output of the
s.a.w.o. must be prescaled in a fixed counter before the
c.m.o.s. variable divider (Fig. 2).

4.2 V.h.f. Synthesizer Performance

The module used a 120 MHz v.h.f. s.a.w.o. incorporat-
ing a readily available L = 350 λ delay line. The long
delay (∼ 3 μs) restricts the number of available channels
in this experimental synthesizer. Prescaling was achieved
in a Plessey SP 8655 emitter coupled logic (e.c.l.) fixed
divider. A c.m.o.s. 4059 counter, which was programmed
from external thumbwheel decade switches, was used for the
variable divide-by-9600. C.m.o.s. phase comparison
and fixed reference division was also used. With a passive
RC loop filter the power consumption, 50 mW, in the
digital control loop arose predominantly from the e.c.l.

prescaler. The oscillator tuned from 119-90 MHz to
120-05 MHz, permitting the synthesis of 12 channels with
12.5 kHz spacing. The prescaling by 32 limits the overall
division ratio of the variable divider, and reduces the
comparison frequency by the same factor of 32, from
12.5 kHz to 390-625 Hz. This restricts both the loop
gain and the tuning time. These performance deficiencies
have resulted in more sophisticated approaches in the
design of the following u.h.f. synthesizers.

4.3 U.h.f. Synthesizer Designs

In a multichannel frequency synthesizer which retains
a low loop cut-off frequency to permit direct modulation
of the s.a.w.o. with the voice input there is a limit to the
minimum oscillator Q. The Q must be sufficiently high
to maintain a narrow oscillator linewidth stopping the
transmitter radiating excessive energy (∼-90 dB) into
adjacent radio channels. This sets a minimum Q value of
∼ 500. Equation (3) subsequently yields the minimum
delay line length as L = 160 λ, and equation (2) gives the
maximum deviation for a 480 MHz s.a.w.o. as 1-5 MHz.
Although this oscillator deviation is low in comparison
with the octave bandwidth of an LC v.c.o., synthesis of
120 u.h.f. 12-5 kHz radio channels is adequate for many
mobile radio applications. In fact, the current band-
width of Pye PF9 u.h.f. pretuned Pocketphones is only
1-5 MHz.

Here two distinct design approaches are reported
which overcome the restricted comparison frequency
when a fixed prescaler is inserted before the variable
divider. Either the new variable dual modulus prescalers
can be incorporated (Fig. 7) or the v.c.o. output can be
mixed with a separate stable oscillator down-converting
(Fig. 8) to frequencies which can be accommodated in
the variable dividers.

The variable prescalers9 are based on e.c.l. counters
which normally divide by a fixed radix, e.g. 10, but in
response to an asynchronous input from the program-
mapping counter they will count one extra pulse and divide
by 11. Variable prescalers can be cascaded or combined
with fixed dividers to form high speed variable radix counters. When followed by conventional c.m.o.s. variable dividers the synthesizer comparison frequency does not require to be reduced as in the 120 MHz synthesizer. The new system (Fig. 7) offers high divider speed and complexity for moderate power consumption. Normally, the loop filter would have difficulty in suppressing the control line ripples introduced by the variable prescaler at subharmonics of the comparison frequency. This is not a problem in the s.a.w.o. synthesizer module as the loop cut-off is purposely kept to low audio frequencies.

Preliminary experiments are now being performed on a u.h.f. synthesizer based on this design concept. The synthesizer incorporates an e.c.l. fixed divide-by-two followed by a variable divide-by-80/81 with the remainder of the control electronics realized entirely in c.m.o.s. circuitry. Loop power consumption of 150 mW is contributed primarily by the e.c.l. prescalers. The edge triggered phase detector provides a lock range equal to the capture range. With a \( L = 200 \lambda \) 480 MHz delay line the synthesizer initially covered 30 channels between 479.8 MHz and 480.175 MHz at 12.5 kHz spacings. The feedback amplifier and phase shifter are now being optimized to obtain the full \( \pm \pi/2 \) phase shift for 96 channel coverage. Detailed measurements will subsequently be performed on synthesizer spectral purity and tuning time.

This synthesizer is limited by the s.a.w.o. deviation to operation in either the transmitter or receiver. With two oscillator delay lines, which are offset in frequency by the radio i.f., and sidestep logic in the variable divider, one synthesizer can operate in both the transmitter and receiver. Alternatively it may be possible with ladder i.d.t. design to operate one multi-moded s.a.w.o. stably at either the transmitter or receiver frequencies.

In the alternative u.h.f. synthesizer design (Fig. 8) the requirement for the high speed variable prescaler is removed by mixing the u.h.f. v.c.o. output with a separate u.h.f. fixed stable oscillator operating slightly below the minimum v.c.o. output frequency. Low-pass filtering selects the difference frequency which is subsequently divided in the digital control loop. Moderate prescaling may be required dependent on the desired number of channels. This approach for synthesizer design is not presently favoured as any drift or noise on the high stability fixed u.h.f. oscillator is transferred to the v.c.o. Thus, there is an excellent application here for the single-channel phase-locked s.a.w.o. module reported earlier.

In principle, this u.h.f. synthesizer could be implemented with two s.a.w.o.s. One would be used as an intermediate Q u.h.f. v.c.o., while the other would provide the high Q u.h.f. fixed output. However, the enhanced electronic tuning range of the conventional LC v.c.o. is attractive as it permits the synthesizer to be offset by the radio i.f. for use in both the transmitter and receiver. In Fig. 8 the s.a.w.o. operates on a harmonic of the radio i.f., e.g. 23 MHz. On switching from transmit to receive the reference frequency is added to the s.a.w.o. output in a second mixer to introduce an i.f. offset. The v.c.o. subsequently retunes without increasing the operating frequency or incorporating sidestep into the variable divider.

The use of a v.c.o. rather than a s.a.w.o. as the controlled oscillator in this synthesizer necessitates a wideband control loop to improve the low Q v.c.o. short term stability. In addition the large change in loop gain introduced by the variable divider will require careful design of the loop filter if capture is to be maintained at all frequencies. This may require the frequency selection information also to be used to control the loop filter time constants. The selection of an LC v.c.o. or s.a.w.o as the controlled oscillator involves a delicate compromise between tuning range, noise performance and efficiency. The s.a.w.o. offers improved wideband s.s.b. f.m. noise with increased loop power. In contrast the LC v.c.o. is constrained by the varactor diode breakdown voltage which sacrifices tuning range in high power low noise sources.

The synthesizers reported here have predominantly used low cut-off frequencies in the loop filter to permit simultaneous f.m. of the module with audio information. This has the disadvantage that it increases the tuning time to approximately one second. In applications such as the new urban cellular systems, where channel allocations...
are reassigned as the mobile alters its location, the long tuning times will result in loss of information. Here sophisticated design techniques, which increase the comparison frequency above the channel spacing to give a wideband control loop, are required to permit fast synthesizer switching. This will also permit the use of low Q (e.g. 100) s.a.w.o.s with a consequent fivefold increase in the number of synthesizer channels, over that reported here. Normally modulation of this synthesizer with information would have to be performed externally. However, if the audio input is suitably pre-emphasized then it can be modulated within the wideband control loop.

5 Conclusions

The paper has outlined the design of delay stabilized single moded s.a.w.o.s and compared them briefly against existing crystal oscillators. Table 1 highlights the fact that although the s.a.w.o. Q is lower than a crystal oscillator, when operated at high loop power the higher s.a.w.o. operating frequency gives it a noise performance comparable with a multiplied crystal source. The current performance of s.a.w.o.s, which utilize separately packaged delay line and maintaining amplifier, is predicted to improve significantly with the recent development of thin film hybrid s.a.w.o.s (Fig. 9) which minimize connection and packaging parasitics. Direct incorporation of a u.h.f. s.a.w.o. in personal radiotelephone equipments, which must cover a 50°C temperature range with < ± 3 kHz frequency drift, is currently not possible. Therefore phase-locking techniques were employed to control the s.a.w.o. from a reference crystal oscillator. The demonstrated u.h.f. s.a.w.o. single channel synthesizer module was capable of frequency modulation

![Diagram of synthesizer incorporating SAWO](image)

**Fig. 8.** U.h.f. synthesizer incorporating SAWO.

![Image of hybrid SAWO module](image)

**Fig. 9.** 458-75 MHz hybrid SAWO incorporating custom designed thin-film amplifier.

(Courtesy Hewlett Packard Ltd., South Queensferry)
with greater than 5 kHz deviation without unlocking the loop. Its superior d.c. to r.f. efficiency (Fig. 6) is most significant in battery-powered mobile radio equipments.

The 1–2 MHz frequency deviation of intermediate \( Q \) u.h.f. s.a.w.o.s also permits the design of multichannel frequency synthesizers based on these oscillators, which cover approximately a hundred u.h.f. radio channels. The design and operation of prototype v.h.f. and u.h.f. synthesizers has been briefly reported.

The u.h.f. s.a.w.o. is also applicable in h.f. synthesizers. This can be accomplished by outputting the h.f. difference frequency after the low-pass filter (see dotted output Fig. 8) in place of the u.h.f. output. This immediately overcomes the requirement for controlling the absolute accuracy of the high \( Q \) u.h.f. s.a.w.o. Although a u.h.f. v.c.o. is capable of deviation over the complete 3–30 MHz h.f. band, a miniature, rugged, high power low \( Q \) u.h.f. s.a.w.o. is capable of deviation over \( > \frac{1}{2} \) of the required bandwidth. Coverage of the entire h.f. band could then be obtained by switching the high \( Q \) s.a.w.o. between three separate delay lines, to achieve a low noise, s.a.w.o. based, h.f. synthesizer.

The recent development of multi-moded s.a.w.o.s\(^{3,13} \) will extend considerably the number of radio channels which can be covered by s.a.w.o. based frequency synthesizers. Stable, single-moded operation\(^ 2 \) can be obtained by exciting these oscillators with a short r.f. pulse\(^ 3 \) or by combining two s.a.w. oscillators.\(^ {13} \) Multi-mode synthesizers do require more hardware than those reported here and the synthesis of 12-5 kHz channels requires an 80 μs (30 cm long) delay line. However, they do promise a considerable extension to the tuning range of s.a.w.o.-based synthesizers in the near future.

A most significant development is a new oscillator\(^ {16} \) employing conventional s.a.w. i.d.t.s to generate and detect a surface skimming acoustic wave. When compared to the s.a.w.o.s reported here it promises increased operating frequency plus vastly improved temperature performance and the insensitivity of bulk wave propagation to surface contamination should give oscillator ageing rates comparable with conventional crystal controlled oscillators.

## 6 Acknowledgments

The authors wish to acknowledge the loan of 120 and 460 MHz delay lines from Hewlett Packard Limited, and 480 MHz delay lines from the Marconi Research Laboratories. The assistance of colleagues here in the department and helpful discussions and suggestions with various industrial companies is also gratefully acknowledged. These studies were sponsored by the British Science Research Council.

## 7 References