THE FORMING PROCESS IN AMORPHOUS SILICON MEMORY DEVICES

by

W. K. Choi

A thesis presented for the degree of Doctor of Philosophy

Faculty of Science

University of Edinburgh

May, 1986
DECLARATION

This thesis is the original composition of the author's work, unless stated otherwise, and has not been submitted previously for any other degree.
DEDICATION

To my parents, especially on my father's 60th birthday.
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ACKNOWLEDGEMENTS

I would like to thank my supervisor Professor A.E. Owen for his patience and unfailing support given throughout this work. I would also like to express my sincere thanks to Dr. J. Hajto and Dr. S Reynolds for their help and thought provoking discussions during the last three years. I am also indebted to Dr. S. Reynolds for his meticulous proof reading.

I am grateful to Professor W.E. Spear FRS, Dr. P.G. LeComber and the technical staff of the Carnegie Laboratory of Physics, University of Dundee for providing the amorphous silicon samples used in this project. Special thanks are also due to Professor W.E. Spear and Dr. P.G. LeComber for many useful discussions and for making available some of their unpublished data which has been included in this thesis.

I am ever indebted to my good friend, Joaquim J. Delima for many fruitful hours spent in discussing the physics of thin films.

The useful discussions with Dr. N.L. Sims, Dr. G.B. Scott and Dr. P.J. Hockley of B.P. Research Centre, are also gratefully acknowledged.

I am honoured to have been awarded an Edinburgh University Studentship and am grateful for being allowed the use of their laboratory facility.
I would also like to acknowledge the help of my friends, Dr. N.W. Kour, Dr. A.M. Al-Saie, Mr. I.M. Flanagan, Mr. S. Gage, Dr. A.J. Snell, Dr. A.P. Firth and other members of the Material and Devices group.

Finally I would also like to express my sincere gratitude to my parents and my sister Miss H.P. Choi for their understanding and encouragement.
The forming process of glow discharge (GD) deposited amorphous silicon (a-Si:H) p⁺-n-i devices has been studied. Results on the basic electrical characteristics of the virgin state (i.e. before the device is formed) and the ON- and OFF-states (i.e. in the formed device) are also included to provide a better understanding of the forming process.

It was found that in the virgin state there is a critical n-layer thickness \( d_{nCR} \) where p⁺-n-i devices with n-layer thickness \( d_n \) less than \( d_{nCR} \) behave like a p⁺-i structure. The same conclusion has also been reached from capacitance-voltage measurements. The current-voltage (I-V) characteristics of p⁺-n-i structures with \( d_n > d_{nCR} \) at moderate forward bias can be analysed using the one-carrier space-charge-limited current (SCLC) model. The trap density derived from the one carrier SCLC model for the n-layer is close to the density of the gap states reported in the literature. At still higher voltages the I-V characteristics become dominated by a Schottky barrier and this region leads directly into forming.

Current instabilities in the virgin state, and other processes leading to forming, may be related to a charge storage mechanism similar to that proposed for the crystalline silicon (c-Si) metal-
insulator-semiconductor-semiconductor (HISS) structures. However, a detailed comparison with the theories developed for the c-Si HISS devices proved unsatisfactory. It would be useful if these models could be adapted to take account of the amorphous nature of the present devices.

There is clear evidence for filamentary conduction in the ON-state, after forming, but current flow seems to be uniform across the device area in the formed OFF-state. The mechanisms of switching are still not understood however and are the subject of further studies.
Electronic switching and instabilities in thin films of a variety of semiconductors, semi-insulators and insulators were first reported as early as the 1940’s and there is now a considerable literature on the subject. These phenomena usually occur at high fields, often leading to current instabilities and, subsequently, destructive breakdown. In a number of crystalline and amorphous materials however, a current instability is sometimes associated with a negative resistance effect followed by switching, and this can be non-destructive.

Research on thin films remained dormant but after the report of non-destructive (threshold and memory) switching in thin films of certain amorphous chalcogenide alloys in 1968(1), there was an enormous increase in interest in the physics and technology of switching. There are still some controversial features but by and large acceptable models for both threshold and memory switching in chalcogenide glasses are now reasonably well established(2,3).

During the 1960s and early 70s most research in the field of amorphous semiconductors was concentrated on the glassy chalcogenide group of materials, motivated largely by technological interest in their electrical switching properties. In this period there was relatively little activity on amorphous silicon and other amorphous
tetrahedral semiconductors, although Feldman and Woorjani (4,5) and Dey and Fong (6,7) did report threshold switching effects in evaporated amorphous silicon, and amorphous germanium. There was, however, no clear evidence for memory switching. The discovery in 1975 that doped hydrogenated amorphous silicon (a-Si:H) could be prepared by the glow discharge decomposition (GD) of silane and appropriate dopant gas dramatically changed the situation (8). The ability to dope a-Si:H n- and p-type stimulated a vast amount of research on the basic physics and technology of the material. Increasingly intensive research and development, especially in Japan, lead relatively quickly to successful device applications of a-Si:H, e.g. solar cells for hand-held calculators, photoreceptors in electrophotography, field effect transistors as control devices in large-area liquid crystal displays. Despite the wide ranging research on a-Si:H however, threshold and memory switching comparable to that observed in chalcogenide glasses was not reported until recently.

Three papers concerned specifically with switching in a-Si:H appeared almost concurrently in 1982, each reporting very different effects observed in different a-Si structures. den Boer (9) studied $n^+ - i - n^+$ structures of a-Si:H prepared by the glow discharge technique and found that the devices functioned as threshold switches with nonpolar characteristics. He also reported that a "forming" process is necessary for the threshold switching action (the general and specific features of forming will be described and discussed in detail in Chapters 7 and 8). Gabriel and Adler (10)
searched unsuccessfully for switching in r.f. sputtered thin films of homogeneous a-Si:H with molybdenum contacts. They concluded that, unlike chalcogenide glasses, hydrogenated a-Si:H does not have the fundamentally requisite properties for reversible switching behaviour. Owen and co-workers(11) however, reported memory switching in p⁺-n-i structures of a-Si:H prepared by the glow discharge technique and, like den Boer, they also found that a forming process is required before these structures function as memory devices.

The memory device described by Owen et al is an analogue to the crystalline silicon (c-Si) metal-insulator-semiconductor-semiconductor structure (MIS/S), first described by Yamamoto and Morimoto(12). It should be noted that this device is a threshold switch, and generally no forming is required although according to Kroger and Wegener(13), in some c-Si MIS/S devices "forming" does occur. Several models have been postulated to explain the switching mechanisms in c-Si MIS/S devices.

This work is a study of the switching phenomena in a-Si:H memory devices with special attention focused on the forming process. Results on the basic electrical characteristics of the virgin state (i.e. before the device is formed) and on the ON- and OFF-states (i.e. in the formed device) are also included to provide a better understanding of the forming process.

In the next chapter, a discussion of the transport properties and device physics of glow discharge deposited a-Si:H will be
presented. This is followed, in Chapter 3, by a review of non-ohmic high field effects in homogeneous semiconductors, which are often a precursor to switching or breakdown in thin films. Chapter 4 develops from Chapter 3 in describing different types of switching phenomena in homogeneous semiconductors, with particular emphasis on a-Si thin films. Switching in c-WISS devices is considered in detail in Chapter 5, to serve as a comparison to its amorphous counterpart. The experimental techniques, including the fabrication of the amorphous memory devices, are outlined in Chapter 6. Experimental results are described in Chapter 7 and discussed in Chapter 8. Chapter 9 summarises the work and concludes with some suggestions on areas which the author believes require further work.
References


CHAPTER 2

AMORPHOUS SILICON - AN INTRODUCTION TO TRANSPORT PROPERTIES AND DEVICE PHYSICS

§2.1 Methods of preparation

Amorphous silicon (a-Si) can be obtained by various methods, such as thermal evaporation under vacuum, r.f. sputtering and glow discharge (GD) decomposition of silane. Thin films of a-Si prepared by thermal evaporation and r.f. sputtering tend to contain a high density of defect states and are thus insensitive to doping with either tri- or pentavalent elements. On the other hand, doping with boron or phosphorus is possible in thin films of a-Si prepared by the GD technique.

Doping can be realised in GD a-Si because residual hydrogen saturates the dangling bonds which would exist in the pure amorphous material. This is in contrast to a-Si prepared by thermal evaporation in vacuum or r.f. sputtering of a polycrystalline target where hydrogen gas is absent; consequently doping is not possible in films prepared by these methods, although some workers have used r.f. sputtering in the presence of hydrogen, or hydrogen may be subsequently introduced. In §2.3 the electrical properties of films prepared by thermal evaporation and GD technique are described to illustrate the critical dependence of the film quality on the preparation conditions.
Amorphous silicon which contains hydrogen (i.e. normally prepared by the GD technique) is thus called "hydrogenated" a-Si, and the symbol a-Si:H is adopted throughout this thesis to differentiate it from non-hydrogenated a-Si films.

§2.2 The band diagram of amorphous silicon

It is well established that the absence of long-range order in the structure of non-crystalline solids gives rise to localized states in the mobility gap of these materials. The strong and often critical dependence of the electronic properties of the amorphous material on the density and distribution of localized states is widely reported in the literature, and of all amorphous materials, a-Si:H prepared by the GD technique has been studied most thoroughly. The density-of-state distribution of a-Si:H has been deduced by many workers using different experimental techniques\(^5\),\(^6\),\(^7\).

The density and distribution of the localized states for GD deposited a-Si:H is shown in figure 2.1(5). It can be divided into the extended states, \(E\), band-tail states, \(T\), and the gap states, \(G\) according to the electronic properties of the states. The mobility gap is usually taken to be \((\varepsilon_c - \varepsilon_v)\) in figure 2.1, i.e. the energy difference between extended states in the valence band and extended states in the conduction band. In the extended states, the effects of random potentials and fluctuations in the interatomic distances and bond angles affect the electronic transport properties of the material. According to Cohen\(^8\), transport of electrons just above
Figure 2.1 Density-of-states distributions for a-Si specimens. Curve 1, GD deposited specimen, $T_d = 520K$; Curve 2, GD deposited specimen, $T_d = 350K$; Curve 3, evaporated specimen. The full lines indicate results obtained from field effect experiments and the arrow on each curve shows the position of the Fermi level. E, extended states; T, tail states; G, Gap states (10).
\( \varepsilon_c \) (or holes just below \( \varepsilon_v \)) in this border region between the band-tail states and the extended states is a diffusive process, similar to Brownian motion. The drift mobility for electrons in this region is given by (9)

\[
\mu = \frac{2m}{3} \frac{ea^2}{h^3} \frac{J}{kT} \frac{a^3}{J} g(\varepsilon_c)
\]

where \( J \) is the electronic transfer integral between nearest neighbours which are separated by a distance \( a \), \( Z \) is the coordination number, and \( g(\varepsilon) \) is the effective density of states just above \( \varepsilon_c \). With plausible values for these quantities, equation (2.1) leads to a range of values from 0.1 to 10 cm\(^2\)V\(^{-1}\)s\(^{-1}\) for the mobility in extended states (10).

Localized states start below \( \varepsilon_c \) and the transition from extended states to localized states is of fundamental importance in the theory of the non-crystalline state. Mott, in his extensive work on this problem, regards the Anderson localization theorem as the key to the understanding of electronic behaviour in amorphous solids (11, 12, 13). Anderson considered a model in which site energies are distributed in a random way over a range \( U_0 \). The essential point is that with increasing \( U_0 \) the ratio \( (U_0/J) \) approaches a critical value at which an electron placed near a given site at \( T = 0 \) will no longer diffuse away and thus become localised. It is assumed that this critical condition is achieved at \( \varepsilon_c \). The band-tail states below \( \varepsilon_c \) are then localised in the sense that the average over these states of a relevant physical quantity, such as
the electrical conductivity, vanishes in a rigid lattice.

The electron band tail states $T$ for a-Si:H lie between $\epsilon_c$ and $\epsilon_A$ in a range of about 0.2eV, as shown in figure 2.1. Although direct measurements such as field effect cannot be extended sufficiently close to the valence band, it is believed that the same tail states should lie above $\epsilon_V$. The existence of the band tail states is a consequence of the lack of long-range order of the non-crystalline material. The extent of the distribution is an approximate measure of the disorder potential $U_0$. In a tetrahedral amorphous semiconductor such as Si, the deeper lying gap states, $G$, are determined by structural defects in the random network, such as dangling bonds or vacancies. The nature of the gap states in a-Si:H has been discussed by Mott et al(14); it has also been suggested by Spear(5,15) that at least some of the states at $\epsilon_X$ and $\epsilon_Y$ could be described in terms of the electronic structure of a divacancy. This will be discussed later (see §2.3.3).

The position of the Fermi level, $\epsilon_f$ for undoped a-Si:H is indicated in figure 2.1 by the arrows. It is determined by the charge distribution in the gap states. For instance, in specimens deposited on a substrate held near 350K (curve 2), $\epsilon_f$ has moved to about 0.85eV below $\epsilon_c$ and the density of states in the minimum has decreased by an order of magnitude compared with that of evaporated a-Si. Further reduction in the density of localised gap states may be achieved by increasing the deposition temperature to 520K (curve 1), thereby permitting sensitive doping of the material.
At $T = 0$, $\sigma = 0$ for the localized tail and gap states but for $T \neq 0$ thermally activated hopping transport can take place. The mobility $\mu(\epsilon)$ at energy $\epsilon$ for this phonon-assisted mechanism is given by:

$$
\mu(\epsilon) = \frac{1}{6} \frac{eR^2(\epsilon)}{kT} \nu_{ph} e^{-2\alpha R} e^{-W/kT}
$$

(2.2)

where $R$, the average hopping distance, depends on the density-of-states distribution and is thus a function of energy. The term $e^{-2\alpha R}$ describes the decay of localized wave functions, with the parameter $\alpha^{-1}$ determining the rate of spatial decay; $\nu_{ph} e^{-W/kT}$ represents the probability per unit time that the localized electron hops to a new site at an energy $W$ above the original one. The hopping mobility at room temperature predicted by equation (2.2) is of the order of $10^{-2} \text{cm}^2\text{V}^{-1}\text{s}^{-1}$ or less, which means that near $\epsilon_c$ and $\epsilon_v$ the mobility drops by two or three orders of magnitude compared with that in the extended states, thereby defining the so-called mobility gap. Thus, in addition to extended state conduction, there are many current paths through the localized states, all of which can contribute to the observed electrical properties but it is likely that one of these will predominate at a given temperature.

§2.3 The electrical and optical properties of glow discharge (GD) deposited a-Si:H

Because of the close relationship between the electronic properties and the localized state distribution in a-Si:H, many experiments have been performed to probe the density and
distribution of these states. A major problem encountered however is the critical dependence of most physical properties on the method of preparation, the conditions during deposition and any subsequent annealing treatment.

A-Si can be obtained by various methods, such as the GD of silane(1,10), thermal evaporation under vacuum(2) and r.f. sputtering(3). This project is concerned only with a-Si:H prepared by the GD technique, and hence only electrical and optical studies on that form of a-Si:H will be considered in this section. The influence of localised states on transport properties will also be discussed.

§2.3.1 Electrical properties of GD deposited a-Si:H

The correlation of the basic d.c. electrical properties of intrinsic a-Si:H with different deposition temperature is shown in figure 2.2(15). One important feature is the conductivity minimum at \( T_d = 350K \) (figure 2.2(a)). For specimens deposited above this temperature, the current at room temperature is predominantly carried by electrons, as evident from the drift mobility measurements(16), the sign of the thermopower(17) and field effect(5,18). The magnitude of the pre-exponential factor \( \alpha_0 \) (figure 2.2(c)), is fairly conclusive evidence that the electron transport takes place in the extended states above \( \varepsilon_C \). The observed activation energy \( \varepsilon_0 \), plotted in figure 2.2(b), corresponds to the position of the Fermi level below \( \varepsilon_C \), i.e. \( \varepsilon_0 = (\varepsilon_C - \varepsilon_f) \). Drastic
Figure 2.2 Correlation of the electrical properties of a-Si:H specimens prepared by glow discharge decomposition. $T_d$ is the deposition temperature for GD deposited films. (a) room temperature conductivity $\sigma$; (b) activation energy $\epsilon$; (c) pre-exponential factor $\sigma_0$. (15)
changes occur in specimens deposited just below 350K, when \( \varepsilon_f \) lies at about 0.8eV below \( \varepsilon_C \). The decrease in \( \sigma_0 \) by more than six orders of magnitude indicates that the hole transport is by phonon-assisted hopping(15).

These conductivity results for GD deposited a-Si:H form a fairly consistent picture which, when correlated with other measurements, such as the field effect(5,18), drift mobility(16,19) and the Hall effect(20) lead to a reasonable interpretation. The analysis of the field effect data can be found in reference (5) and the experimental arrangement used to obtain these data is discussed briefly in §2.4.3. The density and distribution of localized states for GD deposited a-Si:H with different \( T_d \), deduced from field effect measurements, is shown in figure 2.3. The full line portions were obtained experimentally and the dotted lines are extrapolations. The results range from the end of the electron tail states \( \varepsilon_a \), approximately 0.18eV below \( \varepsilon_C \), to almost \( \varepsilon_y \) which is associated with the hole hopping transport. The results from field effect measurements confirm the deductions from the d.c. conductivity measurements (figure 2.2). Thus at \( T_d = 310K \) hole transport is predominant, whereas at \( T_d = 400K \) and above conduction is by electrons. With increasing deposition temperature the overall density of gap states is greatly reduced but the drift mobility results indicate that this does not have much effect on the tail states between \( \varepsilon_a \) and \( \varepsilon_C \)(16,19).

A relatively low overall density of the localized states
Figure 2.3 Density of state distribution for GD deposited a-Si:H specimens. The energy is measured from $\epsilon_c$ and the position of the Fermi level is indicated by the arrow. Full lines: $g(\epsilon)$ obtained from field effect measurements(5).
makes it possible to dope a-Si:H. Consider the undoped sample with the Fermi level at $\varepsilon_f$. Suppose that a density $N_D$ of substitutional donors is introduced. Practically all the excess electrons will condense into empty gap states, displacing the Fermi level towards $\varepsilon_c$ by an amount $\Delta \varepsilon_f$. The new Fermi level is determined by

$$N_D = N_D^+ = \frac{\varepsilon_c}{\varepsilon_f} \int_{(\varepsilon_f)_0}^{\varepsilon_c} \frac{g(\varepsilon) \, d\varepsilon}{1 + \exp[(\varepsilon - \varepsilon_f)/kT]} + \Delta n(\varepsilon_c) \quad (2.3)$$

In a-Si:H, the increase in the extended state electron density $\Delta n(\varepsilon_c)$ will normally be negligible in comparison to the first term of equation (2.3). This is basically different from the crystalline case, where in the exhaustion range the density of ionised donors $N_D^+ = \Delta n(\varepsilon_c)$. In the amorphous case, changes in the electrical properties are brought about primarily by changes in the gap-state occupation. Figure 2.4 summarise the results (21) which have been obtained for n- and p-type a-Si:H prepared by gas-phase doping in the GD technique. The room temperature conductivity, $\sigma_{RT}$, is plotted against the gaseous impurity ratio, on the right the phosphine to silane ratio for n-type a-Si:H and on the left the diborane to silane ratio for p-type doping. In the centre of the graph, the conductivities of $10^{-8}$ to $10^{-9}$ (Q cm)$^{-1}$ are representative of undoped GD deposited specimens, the properties of which are largely determined by structural defect states in the mobility gap.
Figure 2.4 Room temperature conductivity $\sigma_{RT}$ of n and p-type GD deposited a-Si:H specimens, plotted as a function of the gaseous impurity ratio. For the right-hand curve, this is the number of phosphine to silane molecules in the gas mixture used for specimen preparation. On the left it is the corresponding diborane to silane ratio. The centre refers to undoped specimens.\(^{(21)}\)
It can be seen that on the n-side a minute quantity of phosphine, (\(-6\times10^{-6}\) ppv), increases \(\sigma_{RT}\) by over two orders of magnitude. This clearly supports deductions from field effect measurements concerning the low value of \(g(\epsilon_f)\). With increasing phosphorus doping, curve 1 in figure 2.1 shows that \(\epsilon_f\) moves into regions of higher state density which slows down the rate of rise of conductivity. With a phosphine to silane ratio of \(10^{-3}\) the conductivity approaches \(10^{-2}\) \((\Omega\ cm)^{-1}\), i.e. \(\sigma_{RT}\) has been increased seven orders of magnitude by phosphine doping. A further increase in the impurity level does not seem to lead to higher conductivities.

Turning now to the effect of boron doping, figure 2.4 shows that initially \(\sigma_{RT}\) decreases to about \(10^{-12}\) \((\Omega\ cm)^{-1}\) and this can be understood from the density-of-states distribution. In an undoped specimen, \(\epsilon_f\) lies at about 0.6eV below \(\epsilon_c\) on the n-side minimum. Hole conduction sets in when \((\epsilon_c - \epsilon_f)\) exceeds 0.85eV. Thus the initial boron doping pulls \(\epsilon_f\) to the p-side of the density-of-states minimum and the decreasing \(\sigma\) reflects the rapid reduction in the number of electrons at \(\epsilon_c\). At a diborane to silane ratio of \(10^{-4}\) there is an almost vertical rise in \(\sigma_{RT}\) by six orders of magnitude, indicating that hole conduction has taken over. The specimens are then p-type and the observed increase in conductivity mirrors the movement of \((\epsilon_c - \epsilon_f)\) on the n-side.

Thus, the 'intrinsic' conductivity of about \(10^{-12}\) \((\Omega\ cm)^{-1}\) increases to \(10^{-2}\) \((\Omega\ cm)^{-1}\) on both the n- and p-sides of the density-of-states minimum and this corresponds to a movement of \(\epsilon_f\).
of 1.2eV, essentially between the onset of the electron and hole tail states. As pointed out by Spear, it would be difficult to explain the results of doping other than by a model of substitutional impurities, which in most respects is similar to that used for crystalline materials(21). From these results, it has been determined that about a third of the incorporated phosphorus atoms act as donors; the additional valence bonds of the remaining phosphorus atoms are most probably accommodated by the random network. Similar conclusions apply to doping with boron (acceptors).

§2.3.2 Optical properties of GD deposited a-Si:H

As in the case of the electrical behaviour, the optical properties of a-Si:H are also strongly dependent on preparation conditions and hence on the localized state distribution. The steady state photo-response as a function of photon energy measured at room temperature on a series of GD deposited a-Si:H specimens deposited at different $T_d$ values is illustrated in figure 2.5(22). The ordinate represents the number of charge carriers flowing round the circuit for each absorbed photon in the specimen; $i_p$ is the photocurrent and $N_0(1-R)$ denotes the number of incident photons per second corrected for surface reflection.

GD deposited specimens prepared between 500 and 600K are very photoconductive and approach unit quantum efficiency. Loveland et al(22) pointed out that there is fairly convincing evidence that the
Figure 2.5 Spectral dependence of photoconductivity in GD deposited a-Si:H specimens prepared at the deposition temperature indicated. The ordinate represents the number of charge carriers flowing around the circuit per photon entering the specimen. $\alpha$: absorption coefficient for a 500K specimen (22).
photocurrent is carried by electrons above $\varepsilon_C$, in fact the same conclusion was reached by Fischer and Donovan(23). The onset of observable photocurrent occurs for photon energies between 0.6 and 0.8eV, depending on $T_d$. More detailed plots of the data show that this threshold correlates well with the position of the Fermi level deduced from the conductivity measurements on the same specimens. It may therefore be concluded that the onset of photocurrent involves transitions of electrons from just below $\varepsilon_f$ to $\varepsilon_C$.

The photoconductivity curves in figure 2.5 also provide approximate information on $g(\varepsilon)$ between $\varepsilon_f$ and $\varepsilon_v$. The sharp rise of $i_p$ between 0.6 and 1eV correlates with that of $g(\varepsilon)$ in figure 2.1 just beyond the minimum. This is followed by a shoulder between 1.1 and 1.3eV in all the curves, which may well correspond to a local maximum in $g(\varepsilon)$ at $\varepsilon_v$. From the photoconductivity and absorption curves, an optical gap energy between 1.5 and 1.6eV was deduced which confirms the estimation from the electrical measurements. This result is in substantial agreement with values obtained by Grigorovici and Vancu(24) and Lewis(25) for well annealed evaporated a-Si specimens.

Earlier work on the optical properties of the undoped a-Si:H relates the recombination of the photogenerated excess carriers to transitions in the known state distribution(14,22). The advent of substitutional doping in GD deposited a-Si:H made it possible to investigate optical properties, including photoconductivity $\sigma_{ph}$ with the Fermi energy in widely different parts of the state
distribution(26).

Some photoconductivity results on doped and undoped a-Si:H are summarised in figure 2.6. The room temperature photoconductivity normalised to an incident flux of $7 \times 10^{14}$ photons s$^{-1}$ cm$^{-2}$ ($\hbar\omega = 2\text{eV}$) is plotted against the position of the dark Fermi level for a number of phosphorus doped ($\Phi$), undoped (+) and boron doped (o) specimens. The line $P.G. = 1$ refers to unit photoconductive gain at the comparatively moderate applied field of $3 \times 10^3$ V cm$^{-1}$ used throughout. The interesting result is that slight phosphorus doping (about 10 vppm of phosphine) causes a rapid increase in $\sigma_{ph}$ and the recombination lifetime increases by one to two orders of magnitude. At this stage the recombination also changes from a predominantly monomolecular to a bimolecular process, as is indicated by curve $\nu$ representing the exponent in the intensity dependence $\sigma_{ph} \propto I^\nu$. On the other hand, slight boron doping, which moves the dark Fermi level into and beyond the density-of-states minimum, leads to a considerable reduction in $\sigma_{ph}$. The quasi-Fermi levels $\epsilon_{fn}$ and $\epsilon_{fp}$ for electrons and holes were used to describe the modified electron and hole distribution under photoexcitation. Their position is a function of temperature and incident/intensity. For instance, $\epsilon_{fn}$ will move towards $\epsilon_c$ with increasing $I$ and/or decreasing $T$. The occupancy of states above $\epsilon_{fn}$ and below $\epsilon_{fp}$ will depend mainly on kinetically controlled recombination transitions(26). In figure 2.7, the photoconductivity results have been re-plotted against the new variable $(\epsilon_C - \epsilon_{fn})_{T, I}$ for both 295K and 143K. It was concluded that the recombination lifetime attains
Figure 2.6 Photoconductivity at 295 K plotted against $(\epsilon - \epsilon_f)$, the position of the dark Fermi level for phosphorus doped (○), undoped (+) and boron doped (○) specimens. The broken line represents the exponent $\nu$ (see right hand coordinate) in the intensity dependence $\sigma_{ph} \propto I^\nu$. $\sigma_{dark}$ is a typical dark conductivity curve. P.G. ~ 1 refers to unit photoconductive gain at a field of $3 \times 10^4$ V cm$^{-1}$ (26).
Figure 2.7 Photoconductivity at 295 K (right hand coordinate) and at 143K (left hand coordinate) plotted against the steady-state Fermi level position at a photon flux of $7 \times 10^{14} \text{ s}^{-1} \text{ cm}^{-2}$. The broken lines illustrate at each temperature, the exponent in the intensity dependence $\sigma_{ph} \propto I^n$ plotted on a linear scale (26).
its optimum value when $\varepsilon_{fn}$ has moved to a position between 0.35 and 0.3eV below $\varepsilon_c$; at this stage bimolecular recombination also takes place(26).

These results suggest that changes in the charge distribution produced by doping have an important bearing on the detailed photoconductive behaviour. The main aspects of the problem can be summarised in simple schematic form as shown in figure 2.8(26). Diagram (a) shows $g(\varepsilon)$ and suggests that for a typical undoped specimen $\varepsilon_f$ is located by the overlap of two distributions of unspecified defect centres which differ by their charge state. As indicated, this will give rise to tails of acceptor-like, negatively charged states $n_{r'}$, and positive donor-like states of density $p_{r'}$. Diagram (b) illustrates the charge distribution $g$ at low light intensities. The lifetimes of the photogenerated electrons, which are the predominant charge carriers, are determined by capture into the $p_{r'}$ distribution, leading to a monomolecular process. The effect of light phosphorus doping is shown in (c) (for example, $N_D = 5 \times 10^{16} \text{ cm}^{-3}$, which moves $\varepsilon_f$ to about 0.5eV below $\varepsilon_c$). The significant point is that $n_{r'}$ has been increased and $p_{r'}$ decreased by a net total amount $N_D$. Thus doping has removed most of the charged $p_{r'}$ centres which present comparatively high Coulomb cross sections for recombination. As a result, the electron lifetime and the photosensitivity increase rapidly, as is observed in figure 2.6. However, further doping (and/or increased intensity) will move $\varepsilon_{fn}$ and $\varepsilon_{fp}$ into regions of higher state densities and the new charge distribution so produced will set up a competing recombination path.
Figure 2.8 Diagrams for the discussion of the charge distribution in undoped and doped a-Si:H specimens. (a) Density-of-states \( g(\varepsilon) \) plotted against energy. The energy scale is normalized to \( \varepsilon_C - \varepsilon_F = 0.65 \) eV typical of an undoped specimen. \( \rho_r \) and \( n_r \) denote the densities of charged defect centres. (b) Charge distribution \( q \) in an undoped specimen at low light intensities. Recombination is monomolecular; the electron lifetime is determined primarily by transitions to the charged positive centres. (c) Charge distribution with moderate phosphorus doping in the dark or at very low light intensities, \( (\varepsilon_C - \varepsilon_F) = 0.5 \) eV. Reduction in \( \rho_r \) rapidly increases electron lifetime. Recombination still mainly monomolecular. (d) Charge distribution in the doped specimen of diagram (c) illuminated with a higher intensity. Quasi-Fermi levels and demarcation lines are shown. \( \varepsilon_C - \varepsilon_F > 0.33 \) eV so that most negative charge in the system lies in the peak at \( \varepsilon_C \). Bimolecular recombination now takes place between the two regions of charge distribution. (e) Charge distribution in a lightly boron doped specimen at low light levels; \( \varepsilon_C - \varepsilon_F > 0.9 \) eV. Increased density of \( p_r \) centres reduces the lifetime of the excess electrons which still carry most of the photocurrent(26).
This happens at \((\epsilon_c - \epsilon_{in}) = 0.33\text{eV}\); diagram (d) illustrates the distribution and also suggests possible positions for the demarcation lines \(\epsilon_{dn}\) and \(\epsilon_{dp}\). Most of the excess charge in the system is now concentrated in two well-defined regions of the mobility gap (the \(p_r\) distribution is purely speculative) and the new recombination path prevents any further increase of the electron lifetime. It is likely that \(n_r\) and \(p_r\) remain proportional to one another with changes in intensity, giving mainly bimolecular recombination. Finally, diagram (e) illustrates the situation in a lightly boron doped specimen; \(p_r\) is now increased which accounts for the drop in electron lifetime.

\section*{2.3.3 The nature of the localized states}

Having established the basic features of the localized state distribution from both electrical and optical measurements in the GD deposited a-Si:H, a model for the nature of the localized states near \(\epsilon_X\) and \(\epsilon_Y\) was proposed by Spear(5,15). Spear considered a model with dangling bonds in the a-Si:H within the structure rather than the commonly held belief that they are isolated at surfaces. He pointed out that most of the known defects in c-Si are vacancy-associated. The monovacancy is unstable at temperatures above 150K, but the divacancy is a prominent defect centre in Si. It is stable at room temperature and begins to anneal out only above 500K. Figure 2.9 shows the configuration of a divacancy deduced by Watkins and Corbett from extensive ESR studies(27). The two vacancies are at A
Figure 2.9 Configuration of divacancy in Si according to Watkins and Corbett. A, B: original vacancies(27).
and B in the valence bond structure and the model shows how the dangling bonds interact to form molecular bonds, for instance between atoms 2 and 3 and 5 and 6. The states of interest, which also give rise to ESR signals, are associated with the extended orbitals between atom pairs such as 1 and 4.

Photoconductivity studies (28) give the following energy values; a donor at $\epsilon_c + 0.32$ eV, a singly and a doubly charged acceptor state at $\epsilon_c - 0.54$ eV and $\epsilon_c - 0.39$ eV. Because of the similarity in short range order between crystalline and amorphous Si it would be reasonable to expect that the structure and energies should be similar in both cases. It is worth noting that the donor state of the divacancy practically coincides with $\epsilon_x$ and the acceptors now lie fairly close to $\epsilon_y$. If the above agreement is meaningful, it implies that the divacancy should be a satisfactory basic model for the electronic states that arise in vacancy clusters through the interaction of neighbouring unsaturated bonds. As shown by the recombination lifetime calculated from the photoconductivity measurements using the known electron mobility (figure 2.10), the rapid drop in $\tau$ for specimens prepared below about 500K is consistent with the density-of-states picture; the saturation of $\tau$ would possibly be connected with the fact that the divacancy becomes unstable above 500K. However, as pointed out by Spear it would be unreasonable to conclude that a-Si:H is full of divacancies(15); a far more likely interpretation is that multiple-vacancy complexes, which are known to exist in irradiated crystalline silicon, also exist in a-Si:H.
Figure 2.10 Recombination lifetime of photogenerated carriers as a function of deposition temperature of a number of GD deposited specimens (22).
§2.4 Amorphous silicon device physics

§2.4.1 a-Si:H Schottky barriers

The a-Si:H Schottky barrier diode usually consists of a metal-undoped a-Si:H-n^+a-Si:H structure. This structure can be prepared by the deposition of a n^+ a-Si:H layer (approximately 300 Å) on an n^+ c-Si substrate followed by an undoped a-Si:H active layer (approximately 4000 Å thick). Typical I-V characteristics of an a-Si:H Schottky barrier diode are shown in figure 2.11. The forward bias current can be written in the form:

$$J = J_s \left( e^{\frac{qV}{nkT}} - 1 \right)$$

(2.4)

where $J_s$ is the saturation current density, $V$ is the applied voltage, $k$ is the Boltzmann constant, $T$ is the ambient temperature and $n$ is the diode quality factor.

Unlike c-Si Schottky diodes, where current transport is dominated by thermionic emission, Wronski and co-workers argued that due to the short mean free paths of carriers in amorphous materials, the carrier diffusion model of metal-semiconductor barriers is more applicable to the amorphous Schottky barrier than the thermionic theory(29). Deneuville and Brodsky, on the other hand, suggested that the thermionic emission theory should hold to some extent for Pt-a-Si:H diodes(30). Mishima et al reported that from measurements of the a-Si:H Schottky barrier height and its
Figure 2.11 Typical I-V characteristics of a-Si:H Schottky barrier diode (31).
temperature coefficient, the fundamental characteristics of the barrier are better described by diffusion rather than the thermionic emission\(31\). Spear has pointed out that an amorphous barrier (a-barrier) differs basically from its crystalline counterpart in that the net space-charge region in the barrier is determined not only the ionised impurities but also by the localised states\(32\). The barrier profile and properties will depend critically on the density-of-states distribution in the mobility gap of the amorphous material. Hence in an a-barrier formed by metal and n-type a-Si:H, the positive charge distribution in the barrier region will depend on the distribution of localised states and will therefore be a function of both position and energy. Figure 2.12 shows the energy bands in the barrier region of an n-type a-semiconductor in conjunction with a sketch of the density-of-states distribution, \(g(\varepsilon)\), through the mobility gap. The origin for the spatial coordinate, \(x\), lies at the onset of the barrier and the barrier energy \(\varepsilon_b(x)\) denotes the barrier profile and is always measured from energy \(\varepsilon_c\), the onset of the extended states in the bulk of the specimen. The intrinsic Fermi level is denoted by \(\varepsilon_{fo}\) and the Fermi level is shifted to \(\varepsilon_f\) as a result of introducing \(N_D\) donors. The barrier profile is terminated at the metal-semiconductor interface, defining the barrier width \(X = W_o\) in the absence of an applied potential.

To determine the barrier profile requires a knowledge of the space-charge density in the barrier region, and the charge state of the centre is also an important factor. From the interpretation of
Figure 2.12 Energy bands in the barrier region of an n-type amorphous semiconductor. The density-of-states $g(\varepsilon)$ is sketched in the left hand side of the figure (32).
the photoconductive measurements of doped a-Si:H specimens, it was suggested that the $g(\epsilon)$ minimum arises from the overlapping tails of two defect centres which differ by their charge state (see §2.3.2).

The dashed curves in figure 2.8(a) show a likely division of $g(\epsilon)$ into its two components. Division A, extending from the $\epsilon_c$ side into the gap and extrapolated to 1.1 eV, contains acceptor-like states which are neutral when empty, so that below $\epsilon_f$ they will carry a negative charge; their density is denoted by $n^-$. Curve B contains states from the opposite side of the mobility gap which are neutral when full and therefore provide positively charged donor-like states above $\epsilon_f$, density $p^+$. The integrated acceptor- and donor-like charge densities as a function of the Fermi level position in the barrier region has been evaluated at $T = 295K$ using the following equations (32)

\[
n^-(\epsilon_b + \epsilon_c - \epsilon_f) = \int_{\epsilon_c - 1.1eV}^{\infty} \frac{q(\epsilon) \, d\epsilon}{1 + \exp[(\epsilon - \epsilon_c)/kT]}
\]

\[
p^+(\epsilon_b + \epsilon_c - \epsilon_f) = \int_{-\infty}^{\epsilon_c + 0.1eV} \frac{q(\epsilon) \, d\epsilon}{1 + \exp[(\epsilon_f - \epsilon)/kT]}
\]

and $n^-$ and $p^+$ are shown in figure 2.13 by the broken lines. The solid curves in figure 2.13 represent $(p^+-n^-)$ and $(n^--p^+)$, the net positive and negative carriers in localised states lying in a section through the barrier where the barrier height is $\epsilon_b$.

The barrier height can then be determined from this calculated
Figure 2.13 Integrated charge densities in a-Si:H at room temperature as a function of the Fermi level position with respect to the electron conduction path in the barrier region. The full line shows the net charge \((p^+-n^-)\) and \((n^+_p-p^-)\) and the dashed lines \(n^-\) and \(p^+\) separately. The insert clarifies the notation used for the energy (32).
net charge. Consider three sections parallel to the specimen surface shown in figure 2.12. In the shaded area between $\varepsilon_{f0}$ and $\varepsilon_f$ of region 1 which lies in the bulk of the material, the positive charge density $|e|N_D^+$ is balanced completely by the negative density $-|e|(n^-p^+)$ which can be read off directly from figure 2.13 for the appropriate value of $\varepsilon_c - \varepsilon_f$. Section 2 lies in the lower part of the barrier; as compared to 1, the density-of-states distribution shown on the left of the figure has effectively been raised by an energy $\varepsilon_b$ with respect to $\varepsilon_f$. This means that some of the states in the upper half of the shaded region will have changed their occupation, giving a net positive space charge density of

$$\varrho(\varepsilon_b) = |e|N_D^+ - |e|(n^-p^+)(\varepsilon_b + \varepsilon_c - \varepsilon_f) \tag{2.7}$$

in the element. Again $(n^-p^+)$ can be obtained from figure 2.13, but as indicated by the subscript, it is corresponds to $(\varepsilon_b + \varepsilon_c - \varepsilon_f)$. Evidently, once $\varepsilon_b$ exceeds $(\varepsilon_f - \varepsilon_{f0})$, as in 3, the resultant charge in gap state will become positive (see $(p^+ - n^-)$ curve in figure 2.13) so that $\varrho^+(\varepsilon_b)$ now becomes larger than $|e|N_D^+$.

These considerations are summarised in figure 2.14 which shows $\varrho^+/|e|$ plotted against $\varepsilon_b$ for an undoped specimen ($\varepsilon_c - \varepsilon_f = 0.65$eV), an n-type ($\varepsilon_c - \varepsilon_f = 0.3$eV) and p-type specimen ($\varepsilon_c - \varepsilon_f = 1.05$eV). It is evident that the space-charge distribution in the a-Si:H barrier is basically different from that in the crystalline case, where the space charge density is normally equated to the constant donor (or acceptor) density. The a-barrier calculation was achieved by
Figure 2.14 Net space charge density $\rho/e$ as a function of the barrier height $\varepsilon_b$ for an undoped sample with $\varepsilon_c - \varepsilon_f = 0.65\text{eV}$; a doped n-type specimen with $\varepsilon_c - \varepsilon_f = 0.35\text{eV}$ and a doped p-type specimen with $\varepsilon_c - \varepsilon_f = 1.05\text{eV}$ (32).
solving Poisson's equation using a simple step-by-step method in which the barrier is divided into equal energy interval $\Delta E$. In each of these steps, $Q$ was assumed to be constant in order to solve Poisson's equation directly. The steps are related by the condition that both $\varepsilon$ and $d\varepsilon/dx$ should be continuous at each boundary. Details of the step-by-step calculation can be found in reference (32). Figure 2.15 shows a series of barrier profiles calculated from the $Q(\varepsilon)$ distributions by the step-by-step method. The upper curves for $(\varepsilon_C - \varepsilon_f)$ values between 0.25 and 0.85eV represent n-type depletion layers. The barrier widths and shapes in figure 2.15 differ considerably from those calculated with a constant $Q(\varepsilon)$ as can be seen, for instance, from the dashed curve which represents $\varepsilon_b(x)$ for $(\varepsilon_C - \varepsilon_f) = 0.45$eV with $Q(\varepsilon) = |e|N_D$. The effect of the charge distribution in localised states is particularly evident in the case of the undoped and lightly doped specimens. Consider for instance the profile for the undoped specimen $(\varepsilon_C - \varepsilon_f = 0.65$eV) in relation to figure 2.14. As $\varepsilon_b$ increases from 0 to 0.4eV (that is $(\varepsilon_C - \varepsilon_f)$ increases from 0.65 to 1.05eV), the space-charge density $|e|(p^+ - n^-)$ remains comparatively small, leading to the long, shallow part of the profile. Once $\varepsilon_b$ exceeds 0.4eV, the positive charge density in figure 2.15 begins to increase rapidly, which causes the sharp rise in the profile.

§2.4.2 a-Si:H p-n junctions

Following the realisation of substitutional doping of GD
Figure 2.15 Barrier profile $\xi_p(x)$ calculated by the step-by-step procedure described in ref. 32. The upper curves for $\xi_p - \xi_F$ values between 0.25 and 0.85 ev represent n-type depletion layers. The lower curves for $\xi_p - \xi_F$ between 0.85 and 1.25 ev show p-type depletion layers. The dashed curve has been calculated for $\xi_p - \xi_F = 0.45$ ev with a constant space charge density (32).
deposited a-Si:H, Spear et al produced a-Si:H p-n junctions by successively depositing p- and n-type a-Si:H on a glass substrate (33). The a-Si:H p-n junctions had rectification and photovoltaic properties qualitatively similar to those of a crystalline silicon (c-Si) p-n junction. Subsequent a-Si:H p-n junctions prepared by the GD technique by the Dundee group and other workers have appreciably better rectification ratios and much higher forward current densities. They also exhibit typical breakdown effects in their reverse characteristics, similar to crystalline Zener diodes.

The I-V characteristics of an a-Si:H p-n junction can be written in the form:

\[ I = I_s \left( e^{\frac{eV}{2kT}} - 1 \right) \]  

(2.8)

where \( I_s \) is the saturation current, \( e \) is the electronic charge, \( k \) is Boltzmann's constant, and \( T \) is the ambient temperature. The exponential rise of the forward current has the exponent \( eV/2kT \) rather than \( eV/kT \), suggesting that recombination in the junction region plays a more dominant role than the diffusion limited current considered in the Shockley theory. Although equation (2.8) applies to both c- and a-Si:H p-n junctions, there is an important difference in the electronic structure of the two junctions. It is well known in semiconductor physics that for c-Si p-n junctions, the positive and negative space-charge densities necessary for junction formation are essentially equal to the ionised impurity densities on either
side of the junction. The determination of the junction profile in a-Si:H junctions is requires a different approach(10,32). The main reason for this is that the net charge in the space-charge region is a function of the localised states, as in the case of a-barrier. From the point of view of charge distribution, there is no significant difference between the metal-a-Si:H and a-Si:H p-n junction with the exception that while the space-charge region is in the silicon near the silicon-metal interface for the metal-a-Si:H Schottky barrier, the space-charge region extends into both the p- and n-region of a p-n junction. Some of the results presented in §2.4.1 were again used for the determination of the a-Si:H p-n junction profile. Figure 2.16 represents the n-side of a p-n junction. Consider first a unit area of a section parallel to the device surface at $X = X_1$ in the bulk of the material. The intrinsic Fermi level is denoted by $\varepsilon_{f0}$. The negative charges $A$ in the gap states will be balanced by the positive charges $eN_D^+dx$ of the ionised donors in the element with $N_D$ donors. The situation is different in an element at $X_2$ in the junction region, as can be seen from figure 2.16 the negative charge $B$ is now less than $A$ thus causing a net positive charge density. As a result of this net positive charge density, the potential profile of an a-Si:H p-n junction is determined by the density-of-states distribution. Furthermore, two conditions must be satisfied in order to calculate the a-Si:H p-n junction parameters, i.e:
Figure 2.16 The band diagram represents the n-side of an amorphous junction. It illustrates the formation of the positive space charge in the junction region (at $x_2$) (10).
(i) the positive space-charge on the n-side must be balanced by an equal negative space-charge on the p-side, to preserve the overall neutrality of the junction;

(ii) the amount of band bending must be equal to the difference between $(\varepsilon_c - \varepsilon_f)$ on the p- and n-side.

The charge per unit area $Q$ is calculated as a function of the barrier energy $\varepsilon_b$ for both the n- and p-side of the junction. This is achieved by integrating equation (2.5) over the $Q(\varepsilon_b)$ curves in figure 2.13. Figure 2.17 shows $\varepsilon_b$ as a function of $Q$ for an n-region $(\varepsilon_c - \varepsilon_f)_n = 0.35$eV and two p-regions with $(\varepsilon_c - \varepsilon_f)_p = 1.05$ and $1.25$eV. In a barrier height of $0.7$eV, (i.e. with $(\varepsilon_c - \varepsilon_f)_p = 1.05$eV), the vertical line AB in figure 2.17, which is equal in length to this energy, will not only satisfy the two aforementioned conditions but also give the barrier heights on the n- and p-sides of the junction. From figure 2.17 the barrier heights of the n- and p-side are equal to $0.435$eV (at A) and $0.265$eV (at B) respectively. Figure 2.18 illustrates the complete junction profile of this particular a-Si:H p-n junction constructed by this method. In this figure, the x-origin has been chosen to coincide with the interface between the p- and n-type materials and the origin for the energy axis with $\varepsilon_c$ in the unperturbed n-type material. The total width of this barrier is $1040\text{Å}$ of which the greater part ($720\text{Å}$), lies on the n-side.

Similar calculations can be made for p-n junctions with other
Figure 2.17 The barrier height $\varepsilon_b$ as a function of $Q/e$, the integrated charge per unit area for an n-type layer, with $\varepsilon_- - \varepsilon_f = 0.35$eV and two p-type layers with $\varepsilon_- - \varepsilon_f = 1.05$ and 1.25eV. The vertical lines AB and A'B' are used to determine the barrier heights as described in section 2.4.2(32).
Figure 2.18 Calculated barrier profiles of three p-n junctions for the following values of \((\varepsilon_c - \varepsilon_a)\) and \((\varepsilon_c - \varepsilon_d)\): curve a, 0.35 and 1.65 eV; curve b, 0.35 and 1.25 eV; curve c, 0.18 and 1.15 eV. The insert illustrates the choice of origin and the positions of the bands with respect to this point (32).
p, n doping levels. The very narrow p-type barrier in figure 2.18 curve (b) arises when $\varepsilon_f$ for the p-material lies 1.25eV below $\varepsilon_c$ in a region of high-state density. This curve may be considered as the amorphous analogue of the 'One-sided' crystalline junction. If the n-side is also highly doped, then both sides of the junction are narrow, as shown by curve (c) which has a total width of only 330Å.

§2.4.3 a-Si:H FETs

The field effect measurements(5,15,17) designed originally for the determination of the density-of-states distribution, $g(\varepsilon)$, of a-Si:H made a significant contribution to the development of a-Si:H devices (see §2.2 & 2.3). A device which makes use of the field effect is the a-Si:H field effect transistor (a-Si:H FET), and which is now being applied to the addressing of liquid crystal matrix displays as an alternative to the thin-film CdSe transistors. The design and characteristics of an a-Si:H insulated gated FET suitable for driving liquid crystal displays were first described by LeComber et al(34). Since then many workers had entered this field and many papers had been published on a-Si:H FET and its possible applications(35-40).

In this section only the basic device physics of the a-Si:H FET will be presented. The technological aspects of this device, i.e. its possible applications and various methods for optimising device performance can be found in the references quoted above. The basic working mechanisms of c-Si and a-Si:H FETs are similar, and it is
therefore worthwhile to briefly discuss the working mechanism of the former. In c-Si there are two types of device which utilise the field effect i.e. the junction field effect transistor (JFET), the insulated gate field effect transistor (IGFET). The a-Si:H FET is an IGFET device.

The c-Si IGFET can be further divided into two types, the enhancement mode or the depletion mode device. Details of the working mechanisms of these devices can be found in semiconductor device physics textbooks (see for example reference (41)). To facilitate easy discussion of the physics of c-Si and a-Si:H FETs, the working mechanism of an enhancement mode n-channel c-Si FET will be considered. The schematic diagram of the enhancement mode FET is shown in figure 2.19. When a positive bias $V_G$ is applied to the gate $G$, it induces negative charges which will accumulate at the substrate-insulator interface. If $V_G$ is equal to a certain threshold voltage, $V_T$, the induced negative charge in the silicon surface will provide a conducting path which links the source (S) and drain (D) electrodes thus causing a ON-state condition between source and drain. Increasing $V_G$ beyond $V_T$ causes the source-drain current to increase rapidly. A schematic $I_D$ versus $V_G$ characteristic is shown in figure 2.20.

The schematic diagram of the a-Si:H FET and its energy band diagram are shown in figure 2.21. The field effect structure used in the density-of-states measurements is depicted in figure 2.21(a). The a-Si:H film is deposited directly onto a thin (~170 μm) quartz
Figure 2.19 A schematic diagram of enhancement mode XGFET(41).

Figure 2.20 The transfer characteristic of an enhancement mode IGFET(41).
Figure 2.21 (a and b) Specimen geometries used in the field effect experiments. S, D and G represent the source, drain, and gate electrodes; Q is a thin quartz dielectric. (c) Band diagram showing the formation of an electron accumulation layer near the surface between $x=0$ and $x=\lambda$. The electric field $\varepsilon$ from the positive gate electrode induces a charge $-q$ in the a-Si:H. The tail states distribution T5 between $\varepsilon_c$ and $\varepsilon_A$ is likely to limit the band bending at the surface (5,37).
substrate Q, which also acts as the dielectric across which the external field is applied. The other surface contains the narrow gate electrode G, which is carefully aligned with the gap between the source and drain electrode S and D, deposited on the free surface of the a-Si:H film. The main disadvantage of using the quartz substrate as the dielectric is that in order to achieve a sufficiently high electric field, large gate voltages are necessary, which renders such a device unsuitable as a practical switching element. This can be overcome by using a thin-film insulator, which may be prepared as follows. A thin film insulator (\( \leq 1 \mu m \)) of amorphous silicon nitride (a-SiN) is deposited by the GD process (e.g. by using a mixture of silane and ammonia) onto a substrate which carries the evaporated gate electrode G. The a-Si:H is deposited directly onto this SiN film, and source and drain electrodes are deposited on the surface of the a-Si:H film as shown schematically in figure 2.21(b). As described earlier, by applying a voltage \( V_G > V_T \), the induced charges (electrons) accumulate at the a-Si:H-a-SiN interface, providing a conducting path which turns the device ON. Several \( I_D \) versus \( V_G \) plots of early a-Si:H field effect devices are shown in figure 2.22. The striking feature of the curves is the increase in \( I_D \) by over three orders of magnitude for two of the specimens, which occurs when \( V_G \) is made positive. As illustrated in figure 2.21(c), this means that the extended electron states above \( \varepsilon_C \) are pulled toward the Fermi level \( \varepsilon_F \) in a region that extends from the a-SiN/a-Si:H interface at \( x = 0 \) to \( x = \lambda \) in the a-Si:H film; \( \lambda \) is generally between 100 and 1000Å depending on
Figure 2.22 Examples of early field effect curves of $I_D$ versus $V_G$. (1) and (2) refer to specimens prepared at a substrate temperature of about 300°C; (3) and (4) were deposited at 200°C. $O'$ denotes the approximate flat-band position.

Figure 2.23 Transfer characteristics of a-Si:H FET element. The drain current $I_D$ is plotted against the gate voltage $V_G$ for three-drain potentials $V_D$(36).
the values of $V_G$ and $g(\varepsilon)$. The charge $-q$ induced capacitively in the a-Si:H consists mainly of electrons condensed into localised gap states which have been moved below $\varepsilon_f$ when $V_G$ is applied to the gate electrode. As a result the increase in $I_D$ should be largest for specimens with the lowest $g(\varepsilon)$ in the energy range probed. This applies to curves (1) and (2) in figure 2.22, corresponding to specimens deposited at a substrate temperature of about 300°C. It is also likely that for those specimens with low $g(\varepsilon)$ the levelling of $I_D$ at around $10^{-6}\text{A}$ is caused by $\varepsilon_f$ approaching the onset of the rapid rise in the localised tail-state distribution at $\varepsilon_A$, as indicated in figure 2.21(c). Curves (3) and (4) were obtained from specimens deposited at 200°C, which undoubtedly possess a higher overall density of gap states.

It is also worth pointing out that with the introduction of SiN as the insulating layer, as shown in figure 2.23, the a-Si:H FET can be operated at voltages below 15V, so that it is compatible with modern integrated circuit voltage levels. It has also been established that conventional photolithographic techniques, widely used in the semiconductor industry, can with minor modifications be applied to a-Si:H thin film devices. Recently the characteristics and properties of the a-Si:H FET have been studied and efforts have been made to optimise the device performance.

In addition to the a-Si:H based devices described above, there are also a considerable number of switching devices which have been reported in the literature. These will be discussed in detail in
Chapters 4 and 5.
References


(11) Mott, N.F., Phil. Mags., Vol. 17, 1968, 1259


CHAPTER 3

NON-OHEIC HIGH FIELD EFFECTS IN HOMOGENEOUS SEMICONDUCTORS

§3.1 Switching in thin films

If an increasing electric field is applied to thin films, an unstable situation will eventually arise where the rate of energy input exceeds the capacity of the system to dissipate it and this often leads to breakdown. In some circumstances breakdown may lead to a highly conducting ON-state, which requires a small holding current and voltage to sustain it. The original high resistance, or OFF-state, is recovered if the sustaining voltage is removed. In other cases it is possible to establish a permanent ON-state that persists in the absence of any applied voltage, but the OFF-state may be recovered by the application of a suitable current pulse. These two cases of reversible breakdown are termed as threshold and memory switching respectively, and will be described in detail in Chapters 4 and 5.

Irrespective of whether or not high field breakdown in thin films leads to switching, the conditions leading to the electrical instability can usually be formally described by an energy-balance equation(1,2)

\[ A(T,E,\alpha) = B(T,\alpha) \]  

where A is the rate at which energy is gained from the field E at
temperature T and B is the rate at which it is absorbed or dissipated. The parameter α is introduced to denote any other relevant property of the current carriers pertinent to particular situations.

The variation of the two sides of this energy-balance equation will generally be as shown in figure 3.1 in which the abscissa represents some appropriate parameter such as temperature T, energy ε, or injected charge Q_{inj}. The rate of gain of energy from field will normally be given by

\[ A = \sigma(T,E) E^2 \]  

(3.2)

or some straightforward variant of this; the conductivity \( \sigma(T,E) \) is generally a function of temperature and field. With a sufficiently large conductivity that is very temperature dependent, the dielectric will heat up through Joule heating and thermal processes dominate. Thus in figure 3.1 the abscissa represents temperature and the field \( E_2 \) would be the point at which instability sets in. It is worth noting that for a thermal instability, it is not necessary that the conductivity be a function of field(4). The isothermal conductivity may be ohmic at all times, but the dynamic conductance will not remain constant because of Joule heating. Thermal switching is further discussed in §3.2.

Many other conditions of instability initiated and/or sustained by electronic means may also lead to switching. One of these conditions can be, for instance, the double injection of
Figure 3.1 Schematic representation of solutions to the general energy balance equations (3).
charge with recombination where the energy input is stored in the film as injected charge $Q_{\text{inj}}$ (i.e. the abscissa of figure 3.1) or is lost through recombination. Thus we can describe the condition of electrical instability, whatever its origin, in terms of a diagram such as figure 3.1. This will normally be preceded by a region in which the conductivity is field dependent (non-ohmic). What follows, i.e. breakdown or switching, depends upon the properties of the films and on the presence, or absence, of a suitable positive feedback process in the system. In the following sections, instabilities associated with non-ohmic high field effects and Joule heating will be discussed.

§3.2 Joule heating effect

The I-V characteristics of thermal switching and breakdown events in a uniform specimen are illustrated in figure 3.2. Such events arise when the Joule heat dissipated in the device causes a significant temperature rise in the specimen and when the electrical conductivity increases, e.g. exponentially with temperature. Thermal events have been observed in the $10^3$ V/cm range of fields and may probably be experienced outside this range also(5). The characteristic(a) of figure 3.2 illustrates such effects in a typical $10 \ \Omega$ cm GaAs(6) specimen and (b) is typical for an evaporated silicon dioxide(7), or a silicon nitride film(8).

The development of the process may be followed along the characteristic(a). For increasing fields the characteristic is
Figure 3.2 The J-E characteristics of thermal switching process. Detail information see text(6,7,8).
ohmic initially and there is no significant temperature rise. Once the rise become noticeable, the characteristic bends upwards and current grows exponentially with temperature rise in the specimen. The effect of Joule heat is countered by heat transport from the specimen, which increases roughly linearly with temperature rise. When there is no series resistor in the test circuit, the two effects balance each other only up to the maximum voltage, and, at a higher voltage, current runaway occurs. With a suitable series resistor between source and specimen, states in the negative differential resistance part of the characteristic may be established.

The temperature rise at the maximum voltage is in many substances a few tens of degree Celsius. The temperature continues to rise along the negative differential resistance part of the characteristic towards a destructive value. The development of the process along characteristic (b) is the same as along characteristic (a), but there is a difference in the slope of the curve. This is due to the quasi-exponential increase of the electrical conductivity with field in case (b), which often becomes significant at fields above $10^5$ V/cm.

The thermal switching, or breakdown field can be calculated, but rigorous analytical solutions are available for simple situations only. Analytical results are based on the solution of the equations of conduction of heat and of current continuity for the specimen, for given temperature and field relations of the
electrical and thermal conductivity of the substance. In general, two extreme geometrical situations have been considered for the calculation of thermal instability. In the first, treated by Wegener(9), the specimen is plane parallel, approximated by a thin film capacitor on a substrate. The current and heat flow in the specimen, perpendicular to the substrate are uniform and so is the temperature. Secondly for a cylindrical geometry, the current flows axially, but the heat radially and temperature and current density are non-uniform and largest at the axis, forming a current filament. Thermal switching has been observed, for instance in chalcogenide switches with electrode separations of 10μm or more, and the threshold conditions quantitatively predicted from a solution of the thermal energy balance equations in a one-dimensional form with conductivity expressed only as a function of temperature, i.e. \( \sigma = \sigma(T,E)(4,10) \).

§3.3 Isothermal non-ohmic effects

Instabilities arising in the non-ohmic, i.e. negative resistance region may be thermal in nature as discussed in §3.2, or electronic, i.e. connected with changes in space charge, carrier lifetime, rate of impact ionisation and/or other properties. The electronic switching process usually occurs at relatively low current densities and at low fields in the range \( 1-10^4 \) V/cm(5). The input power at the occurrence of instability is small, and, in contrast to thermal events, no noticeable temperature rise is
normally observed. After switching, the current flow is often found to be restricted to a filament. Several differing processes may cause the switching events, and in the following sections a description of these processes is presented.

§3.3.1 Space-charge-limited Current

The current density versus voltage characteristic (J-V) for a single carrier space-charge-limited current model can be expressed as (11):

$$J = \frac{9}{8} \varepsilon \mu \frac{V^2}{L^3}$$

(3.3)

where $\varepsilon$ is the dielectric constant, $\mu$ is the electron mobility and $L$ is the sample thickness. So for space-charge-limited current to prevail, a region of $J \propto V^2$ should be evident in the J-V dependence. In addition a relationship of the form $V^2 \propto L^{-3}$ should be observed. At low voltages where injected carrier density is less than thermally generated free carrier density, ohmic behaviour is expected (11), i.e.

$$J = e n_0 \mu \frac{V}{L}$$

(3.4)

where $n_0$ is the thermally generated free carrier density. The traps which are responsible for the build-up of space charge can be divided into shallow and deep traps (11, 12). In amorphous materials, a continuous distribution of traps has been considered (12).
detailed treatment of space charge limited current can be found in reference (11).

Milnes and co-workers(13,14) have shown that the J-V characteristic of silicon p⁺-n⁻-n⁺ structures is firstly ohmic, followed by a $J \propto V^2$ range (see figure 3.3). This range is attributed to single carrier space-charge-limited current manifested by injected electrons. Holes are also injected, and at the beginning of the range they may recombine with deep acceptors. Close to the point of instability, holes fill the acceptors and hole transit through the whole specimen then becomes significant. This results in an effective increase in the hole lifetime. In consequence, the space charge relaxes causing instability, the current density increases and the field decreases. Owing to filament formation, possibly at inhomogeneities in doping, a negative differential resistance d.c. range is experimentally not accessible, and a separate high J - low V branch is observed. This branch is mainly determined by a high current density of holes and electrons in the filament. In this branch J is firstly field independent, followed by a range which is determined by two carrier space charge limitation and by ambipolar diffusion radially outward from the filament. Quantitative theories of these switching events have been developed(11,16). Calculation(13,14) of the I-V characteristics for silicon specimens are in good agreement with observations in the ohmic and in the high current - low voltage range, but the agreement in the values of the switching fields was found to be only 'acceptable' (5).
Figure 3.3 The J-E characteristic space charge limited current model (15).
Theories based on the existence of space-charge-limited current have also been used to explain threshold switching in chalcogenide glasses(17). A more detailed investigation has been carried out by Robertson(18) and some of his results for three As-Te-Si glasses are plotted in figure 3.4. Although the data show the expected functional dependence on temperature and thickness, none of the lines in figure 3.4(b) and (c) pass through the origin. This is confirmed by the results of Fagen and Fritzsche(19) as shown in figure 3.4(b). Unlike the case of silicon p⁺-n⁺ structure, Owen and Robertson(3) pointed out that the nonzero intercepts of figure 3.4(b), (c) cast considerable doubt on the applicability of a simple space-charge-limited model for the explanation of threshold switching in chalcogenide glasses. They also point out the lack of the crucial evidence for space-charge-limited current, i.e. the thickness dependence, in most of the interpretation.

§3.3.2 The Poole-Frenkel and Schottky effects

The Poole-Frenkel and Schottky effects have been widely used to interpret the non-ohmic I-V dependence of many amorphous oxide and polymer dielectrics(20,21). Although these non-ohmic phenomena do not necessary lead to switching, they are often a precursor to subsequent instability. In a metal-insulator or metal-semiconductor contact, Schottky emission was observed as a result of electrons being emitted from the metal into the conduction band of the insulator or semiconductor. This effect is therefore associated with

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Figure 3.4 (a) I-V data without Joule heating represented as log resistance (R) versus V for films of different thickness. Measurements made at room temperature (3,19).

(b) Influence of temperature on the slope of lines on a log R versus V graph, e.g. figure 3.4(a), for two thicknesses; x: 0.45μm, o: 1.4μm. Data from Fagen and Fritzche (12) are also plotted for comparison.

(c) Influence of electrode separation on the slope of lines on a log R versus V graph, e.g. figure 3.4(a).

Composition:

(As₂Te₃)₅.5Si₁.5
the barrier at the surface of a metal and the contact material (22). The Poole-Frenkel effect describes the field dependence of conductivity as a result of field enhanced emission from Coulombic centres (23), and is connected with barriers in the bulk material. So both the Poole-Frenkel and Schottky effects result from a lowering of the Coulombic potential barrier by an applied electric field as shown in figure 3.5. However, it is worth pointing out that although the restoring force in both cases is due to Coulombic interaction between escaping electron and a positive charge, the two processes differ in that the positive image charge is fixed for the Poole-Frenkel barrier but is mobile for Schottky emission (see figure 3.6). This results in a barrier lowering twice as great for the Poole-Frenkel effect (24).

For one-dimensional current flow, the Poole-Frenkel effect leads to a field dependent conductivity \( \sigma \) of the form (24):

\[
\sigma = \sigma_0 \exp \left( \frac{\beta \Delta E_d}{rkT} \right)
\]  

(3.5)

where

\[
\sigma_0 = e \mu n_0 \exp \left( -\frac{\Delta E_d}{rkT} \right)
\]  

(3.6)

and

\[
\beta^2 = \left( \frac{3 \epsilon^3}{4 \pi \epsilon_0} \right)
\]  

(3.7)
Figure 3.5 A schematic diagram of (a) The Schottky effect, (b) The Poole-Frenkel effect(24).

Figure 3.6 Restoring force on escaping electron. (a) The Schottky effect. (b) The Poole-Frenkel effect(24).
where $e$ is the electronic charge, $\varepsilon_0$ the permittivity of free space, $E$ the electric field, $\varepsilon_r$ the high frequency relative permittivity, $\mu$ is the carrier mobility, $k$ Boltzmann's constant and $T$ is the absolute temperature. $r$ is a parameter ranging from 1 to 2 depending on the position of the Fermi level (24, 25) or degree of compensation, and $\Delta E_d = E_c - E_d$. From equation 3.5, a linear relationship with slope ($\beta / r k T$) would be expected in a $\ln J$ versus $E^{1/2}$ plot. Figure 3.7 illustrates a plot of $\ln \sigma$ versus $E^{1/2}$ for a $\text{Mo-Si}_3 \text{N}_4$-Al sandwich structure (24). It is often found that the precise value of $\beta$ depends upon the dimensionality of the problem (26) and the position of the Fermi level relative to the various charged and uncharged traps (25).

Owen and Robertson (3) have analysed the pre-switching region of the I-V characteristics of certain chalcogenide threshold switches in terms of the Poole-Frenkel effect. Typical experimental data are shown in figure 3.8. The general behaviour agrees with that expected for the Poole-Frenkel mechanism. A more detailed comparison proved less satisfactory, as demonstrated in figure 3.8(b) and (c), which show that variation of slope with temperature and thickness, respectively. This is perhaps not surprising as Jonscher and Hill (27) have pointed out that true Poole-Frenkel behaviour has been found in only a few cases.

The I-V dependence for Schottky emission is given by (22):

$$J = A^n T^2 \exp \left[\frac{-e\Phi}{kT}\right] \exp \left[\frac{eU}{kT}\right]$$

(3.8)
Figure 3.7 The ln I versus V^{1/2} characteristics of Mo-Si_{3}N_{4}-Al sandwich structure(24).
Figure 3.8 (a) Variation of log conductance versus \( V^{1/4} \) as a function of temperature and film thickness. Composition as in figure 3.4(3,18).
(b) Effect of temperature on the slope of the lines in figure 3.8(a).
(c) Effect of thickness on the slope of the lines in figure 3.8(a).
where $\Phi_B$ is the barrier height, $A^*$ the effective Richardson constant, and $e$ is the electronic charge. Pollack (28) has reported Schottky emission in $\text{Pb-Al}_2\text{O}_3$-$\text{Pb}$ structures. Although no instability or switching was reported, it is interesting to note that a "forming" process was observed. After forming, the current passing through the structure had increased by five orders of magnitude, as depicted in figure 3.9. They suggest that the forming results from the establishment of a positive ionic space charge at the cathode, which decreases the effective barrier height at this interface. The space charge may originate from a migration of Al ions to vacant nearby interstices in the $\text{Al}_2\text{O}_3$ lattice (29).

§3.3.3 Tunnelling

A variety of switching phenomena had been found in metal-metal oxide-metal sandwich structures, and these have reviewed extensively by Dearnaley and co-workers (30), Oxley (31) and Simmons (32). These structures commonly require forming before switching operation can be achieved. Dearnaley and his colleagues (30) envisaged local modification of the dielectric during forming as a prerequisite for subsequent filamentary conduction through the modified dielectric. These filaments may extend from one electrode to the other, and switching can thus be explained in terms of voltage-induced rupture and healing in these filaments. They did not make detailed assumptions concerning the nature of the filaments, except to argue that they would selectively rupture and regenerate as the bias was
Figure 3.9 I-V characteristics of a virgin sample showing the sample growth of current during the forming process. Scope traces were photographed at approximately 10 seconds interval, using a continuously applied full-wave-rectified 60 Hz signal (28).
varied, and that filamentary growth could be initiated at local nonuniformities and associated high-electric fields during the application of the forming voltage.

Thurstans(33) proposed a model in which current transport in the formed state is by electron tunneling between metal particles. Such a model explains the behaviour of the low-bias I-V characteristic as a function of temperature. The particular feature of this model is the explanation of the resistivity memory in terms of the metal-oxide tunneling barrier height(33). It is argued that scattering of electrons into the insulator increases the effective work function of the metal oxide barrier. The persistence of the scattered electrons in the insulator will determine the memory effects. At low temperatures, it is likely that scattered electrons will remain in the insulator, thus accounting for the absence of VCNR after the first application of bias at low temperatures. Under these conditions, a state of low conductivity will be retained until the temperature is again raised and the excess trapped charges removed by cycling the bias. The existence of threshold voltages which depend upon the resistance state and the temperature is thus attributed to the removal of the trapped charges by the electric field at the threshold bias. Other features of the formed state such as electron emission and electroluminescence may also be explained using this model(33).
§3.3.4 Impact ionisation and avalanche breakdown

A variety of effects related to "hot electron" phenomena may lead to the initiation of an instability, negative resistance and switching(3). If the electron density is low, a high energy electron may collide with an atom, instead of another electron, and ionise it producing a hole and two low-energy electrons. These two electrons will, in turn, be accelerated to high energies and ionise more atoms; thus the process can cascade to cause an electron avalanche. Impact ionisation, or any other hot electron effect, is not in itself sufficient, however, to produce negative resistance(3). Crandall(34) has investigated the conditions for Current Controlled Negative Resistance (CCNR), and has shown that a possible feedback mechanism involves the increased screening of the scattering potentials due to the increase in carrier density. The electron scattering decreases, leading to an increase in the average electron energy. The hotter electrons cause more impact ionisation, generating more carriers and making the distribution still hotter. Hence, a higher rate of impact ionisation can be sustained at a value of the electric field that is lower than that required for impact ionisation at low carrier density.

One of the most important manifestations of avalanche breakdown is in the operation of p-n junctions. It provides a limit to diode reverse bias voltages or to transistor collector voltage and has, therefore, been studied extensively. The breakdown is localised and the small regions of avalanche are described as microplasmas. Light
is emitted due to electron-hole recombination. The spatial location
and density of the microplasma can be studied, at least in the case
of p-n junctions(35). The microplasmas are thought to occur at
high-field spots associated with, for example, crystalline defects,
inclusions, non-uniformities in impurity concentration, or other
inhomogeneities.
References


CHAPTER 4

SWITCHING IN HOMOGENEOUS SEMICONDUCTORS

Electronic switching and instabilities in thin films were observed as early as the 1940's on vapour deposited alkali halides(1), silicon dioxide(2), and anodically produced aluminium oxide(3), and there is now a considerable literature on the subject. These phenomena usually occur at high fields, and often lead to current instabilities and subsequent destructive breakdown. In a number of crystalline and amorphous materials however, current instabilities associated with a negative resistance effect and/or switching have been observed(4), and these can be non-destructive. The research on thin films remained dormant but after the discovery of non-destructive switching in thin films of certain chalcogenide alloys(5) in the 1960's, there was an enormous increase in interest in the physics of switching. There is a vast amount of published material, and it is impossible to review it all in detail in this chapter. The aim is to provide a brief summary of the major switching phenomena found in homogeneous semiconductors, especially in a-Si and the possible mechanisms associated with such phenomena.

§4.1 General features of switching in homogeneous semiconductors

A variety of switching and related instability phenomena are
commonly referred to in different materials under the vague heading of "Threshold" and "Memory" switching. These switching phenomena can be systematically classified into five major groups whose current-voltage (I-V) characteristics are shown in figure 4.1(6).

(i) A simple negative resistance device has an I-V characteristic shown in figure 4.1(a) which is retraceable except for some hysteresis if the current is changed too rapidly to maintain thermal equilibrium. An I-V dependence of this sort is sometimes referred to as Current Controlled Negative Resistance (CCNR). An example is the well-known thermistor. By using a small load resistor $R_L$, a negative resistance device can be made to switch from a point (A) where the load line is tangential to the I-V curve to the point of intersection (B) of the load line and the characteristic.

(ii) The negative resistance device with memory has two stable states (see figure 4.1(b)). The first state resembles that of case(i); the second state is usually highly conductive and ohmic. It is established at higher currents and remains without decay. The first state can be reset by increasing the current above a certain value and switching it off rapidly. These effects have been observed in oxides and chalcogenides(7,8).

(iii) The switching device has no stable operating point between the high resistance OFF-state and the conductive ON-state, as depicted in figure 4.1(c). The device switches when the
Figure 4.1 Classification of switching and memory characteristics. (a) Negative resistance device, (b) Negative resistance device with memory, (c) Switching device, (d) Switching device with memory, (e) Voltage controlled negative resistance device with memory (6).

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voltage exceeds a threshold voltage $V_t$. It switches to its original OFF-state when the current is decreased below the holding current $I_H$. This type of switching is found in amorphous chalcogenide glasses\(^5\) and is commonly referred to as 'threshold' or 'volatile' memory.

(iv) The switching device with memory also has two stable states (see figure 4.1(d)). The high resistance state, and the mode of switching resemble those of case (iii). The conducting ON-state, which is established after switching by means of a setting current, remains even if the voltage is removed entirely. The OFF-state can be re-established by a short current pulse of either polarity\(^9\). This type of switching behaviour is sometimes referred to as 'non-volatile' memory.

(v) The Voltage Controlled Negative Resistance (VCNR) device starts in a low resistance state, passes through a voltage controlled negative resistance region, and above a voltage $V_C$ switches to a state of high resistance\(^10\). The I-V characteristic is retraced when the voltage is changed slowly as shown in figure 4.1(e). However, the high resistance state is retained at low voltages when the voltage is reduced rapidly. The initial low resistance state can be re-established by a voltage pulse exceeding $V_A$. A unique feature of these devices is their capability of existing in a large number of memory states of different resistance, depending on the choice of the point $C$ from which the voltage is rapidly reduced.
These five major groups of electronic switching and/or instabilities have been observed in a large number of different materials. For instance, oxide glasses exhibit a variety of both current and voltage controlled negative resistance phenomena, and have been reviewed by Dearnaley et al(11), Oxley(12) and Simmons(13). Switching of types (iii) and (iv) occur in amorphous silicon (see §4.2) and germanium(14) and they have also been found in several crystalline and polycrystalline materials. One of the earliest studies was made by Gildart(15) on \( \text{Sb}_2\text{S}_3 \). In some of these materials, such as \( \text{Nb}_2\text{O}_5 \) (16,17,18), an appropriate forming process and the polarity of applied voltage are important for the setting and reset operations. In transition metal oxide films a forming process is also essential before switching can be obtained. However, thin film switches which utilise the large discontinuous resistivity change occurring in \( \text{VO}_2 \) at the first-order phase transition at 68°C(19,20) have been produced, and these do not required forming.

§4.2 Switching in homogeneous a-Si thin films

§4.2.1 Threshold switching in evaporated a-Si

Feldman and Moojani(14,21) were first to report some cursory observations of threshold switching in homogeneous films of electron-beam evaporated a-Si, a-Ge and amorphous boron, and also some very tentative evidence for memory behaviour. The thickness of
the films used varied between 0.3μm and 1.6μm. Typical values of threshold ($V_{th}$) and substanining ($V_s$) voltages obtained for boron, silicon and germanium thin films are shown in Table 4.1. Variations in both $V_{th}$ and $V_s$ from sample to sample were observed and because of the scatter in the data, Feldman and Poorjani concluded that there was no clear systematic dependence of $V_{th}$ and $V_s$ on the thickness of the films.

Memory switching, similar to that reported in chalcogenide glasses, may also be exhibited by evaporated a-Si(14). According to Feldman and Poorjani(14), this appears to be strictly a local phenomenon involving the formation of conducting filaments which are semi-permanent in nature. There is often visible evidence (under a microscope) of the presence of a filament in the form of a "spot" of damage on the contact surface. Feldman and Poorjani(14) found that the size of the spot increased as the number of switching operations increased. The transition from low to high conductivity is brought about by rapid pulsing with a voltage just below threshold and the transition back to low conductivity by increasing the current in the high conducting state. The threshold voltage $V_{th}$ decreases with increasing temperature and $V_s$ is found to be approximately independent of temperature.

Feldman and Charles(22,23) later proposed a switching model based on measurements of the characteristic switching times, using both single pulses and continuous square wave pulsing, as functions of thickness, resistivity and temperature. This model contains both
<table>
<thead>
<tr>
<th>Element</th>
<th>$V_{th}$ (V)</th>
<th>$V_s$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boron</td>
<td>6.1</td>
<td>3.1</td>
</tr>
<tr>
<td>Silicon</td>
<td>5.7</td>
<td>3.1</td>
</tr>
<tr>
<td>Germanium</td>
<td>5.4</td>
<td>3.9</td>
</tr>
</tbody>
</table>

° The values for Ge are at 77°K while those for B and Si are at 300°K.

Table 4.1 Typical threshold ($V_{th}$) and sustaining ($V_s$) voltages for B, Si and Ge switching devices.
thermal and electronic elements, the importance of each component depending on the sample geometry and thickness, and the pulse rate used in the switching experiment. Experimental data obtained from a-Si and amorphous boron samples are presented in Table 4.2.

Feldman and Charles(23) have used heat sensitive liquid crystals to show that, in their samples there is always a uniform temperature rise over the entire electrode area prior to the formation of a filament. The position of the filament is usually close to the centre of the electrode. When current filaments are located on the electrode edges, the switching does not occur along the load line and switching times, $t_2'$, are longer than listed in Table 4.2.

At high pulse repetitive rates or dc, two separate time constants, $t_1$ and $t_2$ were recorded as a result of a change in the characteristic during the switching transition. The $t_2$ portion falls below the load line and could be caused by a decrease in effective capacitance or increase in inductance. In single pulse measurements, only one time constant, $t_p$, is observed and switching is along the load line. The delay time, $t_d$, is a strong exponential function of overvoltage ($V-V_{th}$); it increases as the sample resistance and/or thickness increases and it is slightly longer at low temperatures. Maintaining a voltage slightly below threshold and increasing the temperature of the sample does not bring about switching; in fact the sample becomes more uniformly conducting and tends to behave ohmically. The recovery time, $t_r$, is shorter at
Table 4.2 Typical sample parameters of boron and silicon amorphous films. The switching times are indicated in figure 4.2, $t_d$ is the time from point D, $t_1$ and $t_2$ are two switching times observed during the transition (D-F) to the stable low resistance state (ON state) at point E. During switching, the initial portion D-E ($t_1$) always followed the load line, while the portion E-F deviated below ($t_2$) or above ($t_2'$) the load line. On the return portion of the curve (F-A), there is a reversible (F-G) and an irreversible spontaneous region (G-B). A recovery time ($t_r$) is associated with the G-B region. At room temperature, the D-E portion was not always observed and the E-F portion then followed a smooth nonload line curve ($t_2''$) as shown in figure 4.2 by the dashed lines. Under pulsed conditions, a single pulse time $t_p$ was associated with the transition from the low- to high-conductivity state (14).

<table>
<thead>
<tr>
<th>Sample (thick)</th>
<th>Temp. (°C)</th>
<th>$V_{th}$ (V)</th>
<th>$I_{th}$ (mA)</th>
<th>$P_{th}$ (mW)</th>
<th>$R_0$ (kΩ)</th>
<th>$C_0$ (pF)</th>
<th>$t_d$ (μsec)</th>
<th>$t_1$ (μsec)</th>
<th>$t_2$ (μsec)</th>
<th>$t_r$ (μsec)</th>
<th>$t_p$ (μsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>300</td>
<td>15.1</td>
<td>0.80</td>
<td>12.1</td>
<td>19.0</td>
<td>25.5</td>
<td>3.6</td>
<td>16.4</td>
<td>45.9</td>
<td>6.10</td>
<td>6.4</td>
</tr>
<tr>
<td>(1.03 μm)</td>
<td>77</td>
<td>16.2</td>
<td>0.15</td>
<td>2.43</td>
<td>133.0</td>
<td>20.7</td>
<td>2.7</td>
<td>9.1</td>
<td>40.2</td>
<td>4.75</td>
<td>5.2</td>
</tr>
<tr>
<td>B (0.97 μm)</td>
<td>300</td>
<td>12.0</td>
<td>3.00</td>
<td>36.0</td>
<td>14.0</td>
<td>2.8</td>
<td>33.0</td>
<td>2.5</td>
<td>7.3</td>
<td>63.7</td>
<td>5.95</td>
</tr>
<tr>
<td>(15% C)</td>
<td>77</td>
<td>12.5</td>
<td>0.11</td>
<td>1.38</td>
<td>115.0</td>
<td>2.5</td>
<td>35.5</td>
<td>2.3</td>
<td>4.4</td>
<td>50.9</td>
<td>5.25</td>
</tr>
<tr>
<td>Si (0.76 μm)</td>
<td>77</td>
<td>7.5</td>
<td>0.15</td>
<td>1.20</td>
<td>49.5</td>
<td>21.0</td>
<td>22.5</td>
<td>3.3</td>
<td>12.9</td>
<td>28.5</td>
<td>6.40</td>
</tr>
<tr>
<td>B (0.74 μm)</td>
<td>77</td>
<td>6.8</td>
<td>0.18</td>
<td>1.22</td>
<td>46.0</td>
<td>19.0</td>
<td>14.0</td>
<td>2.6</td>
<td>5.9</td>
<td>33.2</td>
<td>6.00</td>
</tr>
<tr>
<td>(&lt;0.4% C)</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>
lower temperatures and increases with thickness, and $t_r$ increases following the application of a current in excess of the holding value.

The power, $P_{th}$, as well as the product $t_d P_{th}$, at the switching point is lower at liquid nitrogen temperature than at room temperature. The threshold voltage increases with sample resistance and, regardless of the initial low voltage shape of the I-V curve, the curve at high bias rises steeply and follows an $i=V^n$ dependency ($n > 2$), just prior to switching. The switching transition time under single pulse conditions, ($t_p$), is inversely proportional to the thickness of the sample. Measurements show that $t_p$ is commensurate with the calculated RC discharge type time constant, $\tau_{RC}$, where $C$ is the sample capacitance measured at 1 kHz near the threshold voltage and $R$ is the load plus electrode resistance. The shape of the voltage-time characteristic during the switching transition (C-E, figure 4.2) is exponential as expected from the usual capacitance discharge relation.

A model of switching based on these experimental observations, was proposed by Feldman and Charles(23) and is briefly outlined below. As shown in figure 4.3, current flow is initially uniform throughout the volume of the sample. Conduction is firstly ohmic, and is controlled by Schottky, Poole-Frenkel or space charge limited effects at higher bias. Heating of the sample occurs as a consequence of the current flow and, due to the sample geometry, its interior becomes hotter than either the edges or the electrode.
Figure 4.2 I-V characteristics of amorphous semiconductors, defining the measured switching times(22,23).

Figure 4.3 Postulated switching model in an amorphous semiconductor. (a)Uniform heating, (b)centre hot spot, (c)growth of hot spot, (d)resistance profile, and (e) conducting filament(23).
surfaces. The semiconducting nature of the material causes the hotter portion of the sample to have a considerably lower resistance but the sample is still poorly conducting on account of the low conduction regions near each of the electrodes. The fields near the contacts, $E_1 = \frac{V_1}{d_1}$ and $E_2 = \frac{V_2}{d_2}$ now extend chiefly from each electrode to the edge of the central conducting region. The distances $d_1$ and $d_2$ are probably not equal because of the thermal asymmetry introduced by the substrate. The fields $E_1$ and $E_2$ may become extremely high (with time and/or increasing voltage) and as a result the sample becomes more conducting through avalanche or tunnelling processes at the regions of high field. The displacement charge stored on the sample surfaces may now flow through the predetermined breakdown path and cause a conducting filament to form. The filament is maintained through a thermal process and remains stable until the voltage is lowered but it may change shape by lateral conduction as it becomes hotter or colder. The recovery time, i.e. the time to change back from filamentary to uniform conduction, depends on how much the temperature in the vicinity of the filament has increased.

No precise thickness dependence is included in this model, as the field only occurs across the two high resistance interface regions. These high resistance regions may vary with sample geometry (thickness and electrode area), resistance, material, and pulsing conditions. So depending on the overvoltage, sample geometry and pulsing conditions, this model may be consistent with either almost purely thermal mechanisms for switching or almost
purely electronic mechanisms or a combination of both. A very rapid high voltage pulse will cause chiefly electronic switching, because the fields are sufficiently high for breakdown to occur before any significant temperature rise has developed. A gradual rise in voltage will cause mainly thermal switching, as the sample temperature will increase until the conducting region extends to the contacts.

More recently Dey and Fong have reported threshold switching in a-Si(24,25) films prepared by electron beam evaporation of Si (Purity 9N) onto unheated Corning 7059 glass substrates in a vacuum of better than $10^{-6}$ Torr. A Ti-Si-Ti sandwich structure was used, incorporating Si films of thickness 0.29 - 1.12μm. The electrodes (thickness ~1000Å) were deposited without breaking the vacuum. Among many experimental results presented by Dey and Fong, the pulse repetition frequency dependence of the delay time, $t_d$, was found to have two opposite trends, as illustrated in figure 4.4. Below about 1 kHz, $t_d$ increases as the frequency is increased but is independent of the pulse duration. Above 1 kHz, $t_d$ decreases with frequency and with increasing pulse width. These results led them to propose an electrothermal model to explain the threshold switching phenomena. Although quite similar to the one used by Feldman and Charles(22,23), this electrothermal model was developed more quantitatively to account for the threshold switching in evaporated a-Si. In the initial preswitched state the sample current is more or less uniform but the centre of the sample begins to heat up, eventually becoming the origin of the filamentary channel. Heating
Figure 4.4 Variation of delay time ($t_a$) with pulse frequency. Note that $t_a$ increases with increasing frequency below about 1 kHz. The converse is true for frequencies above 1 kHz (24, 25).
increases the conductivity of the Si, which lowers the field in the centre and increases the fields near the cooler electrodes. As the electrical conductivity becomes field-dependent, space-charge effects appear near the electrodes (figure 4.5(b)). The induced space-charge polarisation distorts the field and the resistance of the sample assumes the profile as shown in figure 4.5(d). The resulting increase in resistance in the vicinity of the electrodes causes a propagation of the heat zone closer to the electrodes, increasing the overall conductivity of the sample and leading to an avalanche condition which eventually causes the film to switch (figure 4.5(e)).

In the low frequency range (1kHz), the areas adjacent to the electrodes get progressively hotter, thereby further reducing the field strength and space-charge injection. However, because of the low frequency the temperature near the electrodes is not adequate to sustain thermal switching or an avalanche conduction process. Thus the delay time increases with frequency as more time will be needed to develop the optimum space-charge conditions. Increasing the pulse width will have little effect if its duration is less than the time constant of cooling. In the high frequency range, the decay of space-charge and other possible relaxation mechanisms are the only means of recovering the OFF-state. Dey and Fong pointed out that although the threshold recovery process can be considered as being due to the decay of the excess carriers out of the filament by diffusion and by direct recombination within the filament(26), so that a minimum carrier concentration sustained by the holding
Figure 4.5 A suggested schematic of the threshold switching mechanism in a-Si films for the low frequency case. (a) Preswitched state with uniform current in the sample, (b) localised heating region (B) at near the centre of the film with space-charge polarizations (A) near the electrodes, (c) Resistance (d) As frequency is increases regions near the electrodes are also heated up reducing the space-charge injections with resulting increase in delay time. (e) Final filamentary channel formation (24, 25).
voltage is necessary to maintain the ON-state, the actual recovery may be due to a combination of several mechanisms.

§4.2.2 Threshold switching in glow discharge deposited a-Si:H

Recently, den Boer (27) reported that a-Si:H prepared by the GD decomposition of silane in a n⁺-i-n⁺ sandwich configuration exhibits threshold switching behaviour. The a-Si:H films were deposited on a substrate at a temperature of 300°C. The i-layer thickness range studied was between 0.5 and 2.5 μm, and the 50 nm thick n⁺-layers were prepared by adding 1% phosphine to the silane. Figure 4.6 depicts threshold switching in a typical, n⁺-i-n⁺ device. The current density versus voltage (J-V) characteristic exhibits ohmic behaviour at low voltages, followed by a J=V² relationship. den Boer interpreted the J-V characteristic in the regime before the rapid increase of current prior to switching in terms of the space charge limited current (28, 29).

Before a device could be used as a threshold switch, a forming process, occurring at 40 -100 V was found to be necessary before switching, at a threshold voltage below this range, could be observed. Investigation of the devices under a scanning electron microscope revealed that a permanent spot several micrometers in diameter was produced as a result of the initial "forming" process. As described in the previous section, such a permanent altered region has also been observed in evaporated a-Si switches and it acts as a nucleus for filamentary conduction. The threshold voltage
Figure 4.6 dc current-voltage characteristic of threshold switch with $L = 5\mu m(28)$. 
tends to increase with increasing thickness of the i-layer, but is also found to be dependent on the forming process. Values ranging from 10 to 35V have been observed. In analogy with other amorphous thin film switches, there is a delay time, \( t_d \) which decreases with increasing overvoltage, \( (V-V_{\text{th}}) \). At small overvoltage \( (<1V) \) the delay times are of the order of 1 millisecond. As \( (V-V_{\text{th}}) \) increases, \( t_d \) tends to level off to about several microseconds as illustrated in figure 4.7. Pulsed measurements at a frequency of 10 kHz indicate that the switches remain stable after more than \( 10^9 \) switching operations. The highly doped layers at both contacts appear to be essential for stable device operation.

den Boer did not present a detailed threshold switching mechanism, but suggested that the onset of filamentary conduction during switching occurs in the permanent altered region. During the forming process the device is locally heated to temperatures above the deposition temperature of a-Si:H and the altered region is likely to have a composition different from the rest of the film because of hydrogen effusion(28,29).

§4.2.3 Memory switching in r.f. sputtered a-Si

In 1982, two papers concerning memory switching in a-Si were published at almost the same time. Gabriel and Adler(30) searched unsuccessfully for switching in homogeneous films of a-Si prepared by r.f. sputtering from a polycrystalline silicon target in an argon or argon/hydrogen plasma. Thin film devices were fabricated with
Figure 4.7 Switching delay time vs overvoltage $V-V_{TH}$ for a device with $L=4.2\mu m$ under pulse conditions ($\alpha=0.5$), $V_{TH}$ was 17.2V(28).
the silicon layer sandwiched between two thin film molybdenum electrodes but none showed any reliable switching behaviour. They concluded that the absence of switching in a-Si, as compared with the chalcogenide switches, is due to the inherent physical properties of a-Si. Chalcogenide glasses have three basic properties which, according to Gabriel and Adler, are crucial to reversible switching:

(1) three dimensional stability of the atomic structure to resist crystallisation;

(2) low conductivity so that thermal instability cannot occur;

(3) the unique chemical bonding configuration which leads to suppression of avalanche dielectric breakdown.

Amorphous silicon-hydrogen alloys fulfill the first two requirements but the apparent absence of reversible switching in a-Si suggests that the third is not satisfied. The major differences between a-Si and the chalcogenide glass are related to the nature and density of the defect centres. Amorphous silicon can have defects with a negative effective correlation energy but the high defect creation energies and relatively low stresses in a-Si result in low densities of localised states. In contrast, the chalcogenide glasses always contain large concentrations of negatively correlated defects. Adler et al(31) proposed a model for switching which emphasises the importance of large concentration of such defects for reversible electronic switching.
Owen et al (32) reported memory switching in GD deposited a-Si:H heterogeneous a-Si junctions (see §5.4) which, together with den Boer's results seems to refute the arguments put forward by Adler (30, 31). This is further confirmed by the most recent report that memory switching may be obtained in thin films of a-Si:H (33), which will be further discussed in §5.4.
References


§5.1 Introduction

Numerous negative resistance phenomena using semiconducting structures have been reported in the literature (1) but Yamamoto and Morimoto (2) were the first to report threshold switching phenomenon in crystalline silicon (c-Si) metal-insulator-semiconductor-semiconductor (MIS) structures. Prior to this work, negative resistance was noticed in an experimental study of gold-silicon (Au-Si) Schottky gate FETs (3). Later studies of two-terminal devices having a Si p⁺-n-i-M structure reported that the negative resistance became more pronounced as compared with the Schottky gate FETs (4). The phenomenon was explained by a mechanism involving avalanche multiplication at the edge of the depletion region of the Au-Si contact without considering the effect of a thin oxide layer (4). Negative resistance was also exhibited by devices in which the n-layer was oxidised thermally. These studies made clear that a naturally grown oxide film on the surface of the n-layer was required before switching could be obtained. Moreover, it was found that the current-voltage (I-V) curves of p⁺-n-i-M and p⁺-n-M structures were very different from each other, particularly in the threshold voltage range, and the p⁺-n-i-M structure shows better switching performance (5).
An example of the $p^+\cdot n\cdot i\cdot n$ MISS devices in its simplest form is shown in figure 5.1(a). An n-type epitaxial layer was grown on top of a p-type substrate. A thin semi-insulating layer, in this case $SiO_2$, was grown on the surface of the n-layer. The MISS structure as shown in figure 5.1(a) is a two terminal device although it can be employed as a three terminal device by making a third contact to the n-layer as shown in figure 5.1(b). Apart from the $p^+\cdot n\cdot i\cdot n$ configuration described here, other device structures such as $n^+\cdot p\cdot i\cdot n$, $n\cdot i\cdot n$ have also been investigated. The most crucial part of the structures is the i-layer. It must act essentially as a leaky insulator, and the most frequently used material for the i-layer is an oxide layer thin enough for a tunnelling current to flow through it ($<40 \text{ Å}$). In addition to $SiO_2$, other materials such as polysilicon, amorphous silicon, silicon oxynitride and silicon rich nitride have been used in this role. The results to be presented in 5.2 are mostly concerned with a $p^+\cdot n\cdot i\cdot n$ structure having an $SiO_2$ i-layer, except where otherwise stated.

§5.2 Experimental characteristics of crystalline silicon MISS devices

§5.2.1 Static I-V characteristics

Typical I-V characteristics for a two terminal device $p^+\cdot n\cdot i\cdot n$ are shown in figure 5.2(2,6). The reverse biased (i.e. a negative voltage applied to the p-doped region in a $p^+\cdot n\cdot i\cdot n$ structure) portion of the characteristic is typical of a reverse biased $p^+\cdot n$
Figure 5.2 The I-V characteristic of two terminal MISS structure (12).

Figure 5.3 Structure of MISS devices and proposed circuit symbols. Diagram also illustrates definitions of base with $d_B$, surface depletion layer width $d_d$ and neutral layer width $d_n$ (7).
junction.

When a positive voltage is applied to the $p^+$-contact (i.e. forward bias) the I-V characteristics comprise a low- and a high-impedance state, separated by a negative resistance region. The high-impedance, or OFF-state, is manifested during the initial voltage application, and the device exists in this mode while the voltage is less than the switching voltage, $V_s$. When the voltage exceeds $V_s$, the device switches rapidly to the low-impedance, or ON-state, and the current increases with little increase in the voltage across the device. The nominal voltage across the device in the low-impedance state is referred to as the holding voltage, $V_H$.

Kroger and Wegener(7) assigned the names "emitter", "base" and "collector" to the terminals of the three terminal MIISS device, as shown more clearly in figure 5.3. These terms are used to emphasise the similar functions performed by these regions and the corresponding parts of a bipolar transistor. The emitter is the semiconductor region on the side of the $p^+$-n junction furthest away from the insulator; the base is between the insulator and the $p^+$-n junction, and the collector is the metal-insulator portion of the device. The threshold voltage $V_s$ changes according to the bias current flowing in third (collector) terminal. Experiments performed on three terminal devices are mostly concentrated on the effects of the base current ($I_B$) on $V_s$ and the delay time $t_D$(2,7,8). The combined effects of $I_B$ and pulse height on $t_D$ are shown in figure 5.4. The mechanism responsible for the suppression of $V_s$ by
Figure 5.4 (a) The threshold voltage $V_s$ as a function of base current $I_B$.
(b) The delay time $t_D$ as a function of $I_B$ for different voltage pulse heights (16).
Iₜ is not yet fully understood but the effects of a bias current on the field strength at the surface of the n-layer and on minority carrier injection in this region are considered to be the main causes of the effects.

§5.2.2 Effect of different i-layer materials

As mentioned earlier the i-layer is a most important part of the device. The resistance of the insulator must not be so high that an inversion layer would occur in a metal-insulator-semiconductor (MIS) structure fabricated from the same insulator, but with no junction present in the semiconductor. However, the insulator must not be so conductive that it would not be possible to support an inversion layer at the "insulator"-semiconductor surface, even under the influence of an adjacent forward biased junction. Table 5.1 lists the properties of some of the insulator materials which have been incorporated in the MIS devices. The comments include the important fabrication procedures and performance properties of devices made with particular insulators.

It is interesting to note that Kroger and Wegener report that some p⁺-n-i-W structures require a forming process while other do not. For instance, devices with SiO₂ or amorphous silicon i-layers, when switched for the first time, show a threshold voltage higher than that observed in subsequent switching cycles(7). No further change in Vₛ is usually observed after the first switching event, which typically reduces Vₛ by about 20%. This forming process is
<table>
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<tr>
<th>Insulator</th>
<th>Thickness range (Å)</th>
<th>Method</th>
<th>Substrate temperature (°C)</th>
<th>Comments</th>
</tr>
</thead>
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<tr>
<td>SiO₂</td>
<td>20-70</td>
<td>Thermal oxidation in dry O₂</td>
<td>350-700</td>
<td>MISIoxide structures yield slightly lower Iₜ than do MISIoxide devices. Devices less reproducible than dry O₂ growth.</td>
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<tr>
<td>SiO₂</td>
<td>20-45</td>
<td>Thermal oxidation in steam</td>
<td>350</td>
<td>-</td>
</tr>
<tr>
<td>SiO₂</td>
<td>30-45</td>
<td>Sputtered</td>
<td></td>
<td>-20-80</td>
</tr>
<tr>
<td>SiO₂:N₂ (index of refraction at 2450 Å = 1.55)</td>
<td>30-90</td>
<td>CVD</td>
<td>700</td>
<td>Highest observed yields in simple structures. Lower Vₜ observed in Multiple device than in Multiple.</td>
</tr>
<tr>
<td>SiO₂:N₂ (index of refraction at 2450 Å = 1.5)</td>
<td>70-900</td>
<td>CVD</td>
<td>700-750</td>
<td>Intermediary intermediate state common. Devices extremely sensitive to surface preparation and sputtering conditions.</td>
</tr>
<tr>
<td>Si (amorphous)</td>
<td>300-9000</td>
<td>Sputtered</td>
<td></td>
<td>-33-150</td>
</tr>
<tr>
<td>Si (polycrystalline layer)</td>
<td>17-25</td>
<td>CVD</td>
<td>150-750</td>
<td>Lowest Iₜ observed; devices extremely sensitive to surface preparation; better devices observed using Mo rather than W evaporation boat.</td>
</tr>
<tr>
<td>Si (amorphous)</td>
<td>20-210</td>
<td>Evaporation from Mo boat</td>
<td></td>
<td>-33-70</td>
</tr>
</tbody>
</table>

Table 5.1 Properties of insulator materials used in MISS devices(7).
believed to result from a permanent filling of deep traps within the insulator or at the semiconductor surface. The original threshold voltage (i.e. the virgin state) has not been observed to be restored by temperature-bias stressing for most structures, therefore these devices do not appear useful as non-volatile memory devices. Certain device structures, for instance devices fabricated using polysilicon as the insulating layer, do not show the forming effect.

Kroger and Wegener also report that certain devices show nonuniform conduction in their low impedance state which they argue is not completely unexpected as the region with the lowest value of $V_s$ will conduct first. The temperature of this region will be raised with respect to that of the rest of the device, and will therefore tend to remain conducting since $V_s$ will be further reduced. Note that this argument falls short of demanding filamentary conduction since the insulator does not have a bulk differential negative resistance (DNR) (9).

The choice of insulator material can also affect the temperature dependence of $V_s$. Figure 5.5 displays $V(T)$ for three different structures having identical semiconductor structures but differing i-layer compositions. A marked temperature dependence of $V_s$ is observed for the devices.

§5.2.3 Capacitance-Voltage (C-V) Measurements

Capacitance-voltage (C-V) measurements have only been made in
Figure 5.5 The threshold voltage $V_t$ as a function of ambient temperature for three different MISS structures, all fabricated from the same silicon material which had the base doping level as indicated (7).
the OFF-state and typical C-V characteristics are shown in figure 5.6(11). The capacitance of the device is the sum of three capacitances in series, i.e. the capacitance of the insulator $C_1$, of the surface depletion layer, $C_s$ and of the p-n junction $C_j$. With negative polarity, the p-n junction is reverse biased and the n-i-n part of the device is in a state of accumulation. In this condition a considerable part of the bias voltage is dropped across the reverse biased p-n junction, $C_j$ is dominant, and the C-V characteristics are similar to those of a reverse biased p-n junction. On the other hand, for a positive polarity $C_j$ becomes large due to forward biasing of the p-n junction, and simultaneously the n-i-n portion goes into depletion regime causing $C_s$ gradually to dominate. Consequently the characteristics show the depletion layer capacitance, in a similar manner to MIS diodes. The changes in the C-V curves with test frequency is considered to be linked to the generation rate of hole-electron pairs in a similar fashion to the C-V characteristics in conventional MOS diodes.

§5.2.4 Schottky barrier devices

Threshold switching has also been observed in n-i-n-M structures which have a Schottky-barrier contact to the n-type base as a metal emitter(7). A Schottky-barrier contact can inject minority carriers into silicon, especially at high current biases(10). The n-i region of the device, with a barrier emitter, and the doping of its n-type base were identical to that of the n-
Figure 5.6 Capacitance-voltage characteristics of a two terminal MISS device. The plus voltage means p-substrate being positively biased.(11).
1-n-p\(^+\) device whose temperature dependence of \(V_s\) is shown in figure 5.5(C). The observed temperature variation of \(V_s\) of the PtSi emitter device is significantly smaller than that of the p\(^+\) emitter, in common with other Schottky-barrier emitters. The explanation of the temperature dependence of \(V_s\) for both types of device will be presented in §5.3.2.

§5.2.5 Effect of varying n-layer (base) doping

Simmons and El-Badry(12,13,14), Kroger and Wegener (6,7,8,15), Buxo et al\(\textasciitilde\) have reported different results obtained from the MISS devices as a function of n-layer doping. Simmons and El-Badry investigated the c-Si MISS devices with an n-layer which is either relatively lightly doped \((N_D < 10^{15} \text{ cm}^{-3})\) or relatively highly doped \((N_D > 10^{17} \text{ cm}^{-3})\). For the lightly doped n-layer devices, they found that the switching voltage, \(V_s\), is a function of the thickness and the doping concentration of the epitaxial layer; the switching voltage increases with decreasing doping concentration and increasing epitaxial layer thickness. They proposed a "punch-through" model for this type of device. For the highly doped n-layer devices, the holding voltage, \(V_H\), is found to be a function only of the doping concentration of the epitaxial layer, the holding voltage decreasing with increasing doping concentration. This was explained by an "avalanche" mode of operation. Buxo et al\(\textasciitilde\), Yamamoto and Morimoto(2) and Kroger and Wegener(6,7,8) proposed another model for the threshold switching phenomenon, arguing that
the multiplication of carriers at the silicon-insulator interface is responsible for the switching. Buxo et al show that the behaviour of c-Si MISS devices with n-layer doping lying between the two limiting cases proposed by Simmons (the "punch-through" and "avalanche" models) cannot be explained in these terms. Details of the different models will be presented in §5.3.

For the devices with a lightly doped base, described by Simmons, the temperature dependence of $V_s$ is rather weak as shown in Table 5.2. Kroger and Wegener, pointed out however that all MISS devices show a decrease in $V_s$ if the ambient temperature $T$ is raised sufficiently. In certain devices $V_s$ is extremely sensitive to $T$ ($dV_s/dT = 1V/°C$) over a certain temperature range(7); other devices have a threshold voltage nearly independent of temperature below 200°C(7).

§5.2.6 Optical excitation of MISS devices

Switching of c-Si MISS devices via optical excitation has also been reported(7,12,17). Three changes occur in the I-V characteristics when intrinsic radiation is applied to the device: a reduction in $V_s$, an increase in current carried in the high impedance state, and for many devices, a decreases in $I_s$, the maximum current before the device switches to the low conducting state. Two experiments have been performed(7) which give quantitative information on the optical suppression of $V_s$. The devices chosen for this experiment had a layer of silicon rich
Table 5.2 The threshold voltage ($V_t$) as a function of temperature(12).

Figure 5.7 Illustrating the influence of voltage pulse height on the switching delay time $t_D$. Curves 1, 2 and 3 correspond to pulses of increasing voltage(16).
silicon nitride (300Å) as the insulator. Under intense tungsten lamp illumination the dark $V_s$ was reduced from 15 V to 7.5 V. With weak fluorescent light $V_s$ was reduced by 0.5 V. Kroger and Wegener (7) explain that the creation of electron-hole pairs by optical excitation will aid the development of an inversion layer at lower collector-emitter voltages, causing a decrease in $V_s$.

§5.2.7 Dynamic characteristics

Dynamic pulse experiments have been performed on the threshold switch to measure the switching and delay time of the device (7, 16, 18). Results obtained by Buxo et al are shown in figure 5.7. When a voltage pulse of magnitude greater than $V_s$ is applied to an MISS switch, the current through the device remains low (essentially the OFF-state current) for a period $t_D$, after which it rises more or less instantaneously to the ON-state current. Figure 5.7 illustrates that for three pulses of different magnitude, as the applied pulse height increases (with respect to $V_s$) the delay time decreases. The shape of the current response appears to be controlled by the internal switching mechanisms of the device and is independent of the external circuit. The delay time $t_D$ in the above case lies in the range $10^{-8}$ to $10^{-5}$ seconds. Kroger and Wegener (7) reported delay times as short as a few nanoseconds or less, but they applied pulses rather greater in magnitude. Adan and Zolomy also used the pulse technique to investigate charge storage effects in MISS structures (18). Typical voltage waveforms across the device
are shown in figure 5.8(a) to (c). The device is driven by a pulse generator in series with a 1 k\(\Omega\) resistor. The initial threshold voltage was 15V for a generator pulse frequency lower than about 300 KHz. In figure 5.8(a) it is shown that when driven by 333 KHz voltage pulse (1\(\mu\)s, 15V) (upper curve) the MISS device turns on after reaching the threshold voltage of 14V (lower curve). Increasing the generator pulse frequency in the 660 to 770 KHz range (figures 5.8(b),(c)) diminishes the threshold voltage, almost to the holding voltage of the device (figure 5.8(c)). Adan and Zolomy concluded that the reduction of the threshold voltage is due to charge storage effects.

5.2.8 Coupled MISS devices

Two-terminal devices in close proximity may interact with each other, i.e. their switching action is "coupled". The simplest example is a linear array, as shown schematically in the upper part of figure 5.9(a) where the metal contacts to the i-layer are, typically, 500\(\mu\)m square and 50\(\mu\)m apart. As shown in the graph the coupling is such that if device 2 is switched on, the threshold voltage \(V_s\) of device 1 is lowered, depending on the current \(I_{d2}\) flowing through device 2. Initially there is a sharp decrease in \(V_{s1}\) (from \(~14\)V to \(~6\)V) as \(I_{d2}\) rises to \(~1\)mA, followed by a slower decrease as \(I_{d2}\) is increased to \(~5\)mA. The other curves in figure 5.9 are explained in the captions. Notice that, as might be expected, the farther away the devices are the smaller is the
Figure 5.8 Dependence of $V$ on driving voltage pulse frequency (upper trace). (a) Vertical: 5V/div, horizontal 1μs/div. A threshold of 14V is shown for about 333kHz. (b) Vertical: 5V/div, horizontal 0.5μs/div. A threshold of 6V is shown for about 666kHz pulse frequency. (c) Vertical: 5V/div, horizontal: 1μs/div. The threshold voltage is reduced practically to the holding voltage (3V) for about 770kHz pulse frequency (18).
Figure 5.9 Dependence of threshold voltage upon currents flowing in adjacent elements. The curve No. 1 represents the dependence of $V_{th}$ of device 1 upon the current $I_{d2}$ flowing through 2. The curve No. 2 and No. 3 show the dependence of $V_{th}$ of respective devices upon $I_{d1}$ flowing through (11).
coupling effect.

§5.3 Switching mechanisms in crystalline silicon MISS devices

Simmons and El-Badry developed two simple electrostatic models based on punch-through and avalanche mechanisms applicable to devices with light ($< 10^{15}$ cm$^{-3}$) and heavily ($> 10^{17}$ cm$^{-3}$) doped n-layers respectively. The experiments of other workers on devices with n-layers having medium doping levels ($\approx 10^{15}$ cm$^{-3}$) do not however fit the models of Simmons and El-Badry. In this section, mechanisms which have been described in the literature will be discussed and the important features will be compared and contrasted with those of the a-Si:H memory switch in Chapter 6.

§5.3.1 Models for devices with lightly or heavily doped n-layer

(a) Punch-through operation

The band diagram of a c-Si MISS device is shown in figure 5.10. With increasing negative voltage applied to the collector contact, a depletion region grows in the n-region under the gate electrode. Electron-hole pairs are generated in the depletion region, the electrons being swept out of the device through the p-n junction and the holes being swept to the oxide-semiconductor interface. If the oxide were thick enough to be impervious to holes, then the holes...
Figure 5.10 Energy band diagrams of the punch-through MISS under forward bias: (a) in the high-impedance state; (b) at punch-through; (c) during switching; (d) in the low-impedance state (12).
would accumulate at the oxide-silicon interface and cause the surface under the n-layer to invert, thus limiting $\Theta_s$ to a value of $\Theta_s = 2 \Theta_n$. Since the insulator is leaky, some holes pass through the oxide and hence, as the voltage increases, the n-region actually goes into deep-depletion rather than inversion, as shown in figure 5.10(a).

Since the current, I, flowing in the device in this mode of operation is simply the current generated in the depletion region, the impedance of the device is of the order of that of a reverse biased diode. The width of the depletion region increases with increasing applied voltage. When the applied voltage reaches $V_s$, the depleted portion of the semiconductor reaches through to the $p^+-n$ junction. This phenomenon is equivalent to punch-through occurring in the base of a p-n-p transistor at high collector voltages. The voltage $V_s$ represents the maximum voltage that can appear across the device. Note that the voltage across the oxide just before punch-through is sufficient to pass only the very small current generated in the n-layer. Thus, immediately after punch-through, the field in the oxide is insufficient to allow the relatively large hole-current injected into the n-section to pass through the insulator. Consequently, the injected holes travel as far as the insulator-semiconductor interface and accumulate there. The build-up of the holes at the interface results in two interacting effects:

1) The n-layer begins to move from deep depletion towards inversion (figure 5.10(c)), the voltage drop is transferred to
the load resistor and causing $\phi_S$ and hence the voltage across the device to decrease.

(ii) The field in the oxide begins to increase, allowing an increasingly larger hole current to pass through the oxide. In this manner a negative resistance region develops in the I-V characteristics of the device, as indicated in the I-V curve in figure 5.2.

Punch-through occurs when the depletion region in the n-layer reaches through to the edge of the depletion region of the $p^+\text{-}n$ junction. The switching voltage $V_s$ is given by (12, 13)

$$V_s = q \frac{(d_n - d_j)^2}{2 \varepsilon_x \varepsilon_0}$$

(5.1)

where $d_n$ is the thickness of the n-layer, $d_j$ is the distance which the depletion region of the $p^+\text{-}n$ junction extends into the epitaxial (n-) layer, $\varepsilon_x$ is the relative dielectric constant and $\varepsilon_0$ is the free space dielectric constant.

As pointed out before, during switching both the width of the depletion region and $\phi_S$ decrease and contraction ceases when the surface potential reaches a value

$$\phi_S = 2\phi_n = 2 \left[ \frac{E_s}{2} - (\varepsilon_c - \varepsilon_{fn}) \right]$$

(5.2)

corresponding to the condition for strong inversion, as shown in figure 5.10(d). During switching the current is limited by the rate
at which holes can be transported through the oxide. In the low-
impedance state, the field across the oxide is very high (> $10^6$
V/cm) and the resulting current through the oxide is an exponential
function of this field. Consequently, a slight increase in the oxide
field results in a large increase in the current flowing through the
oxide, in other words, the oxide is now essentially transparent to
the holes and electrons passing through it and the current flowing
through the device is limited by the p-n junction.

As the voltage is reduced, with the device in the ON-state, the
current will fall until it reaches a minimum value $I_H$ and the device
then reverts to its high impedance state. To understand the reason
for this behaviour, it should be recalled that at low current levels
a significant portion of the current flowing across a p-n junction
is a recombination current and the total junction current, $I_j$
comprises two components, the diffusion, $I_d$ and recombination
current, $I_R$. At a sufficiently low voltage and hence low current
level, $I_j = I_R$ and holes injected from the p$^+$ side of the junction
recombine with electrons in the depletion region of the p$^+$-n
junction, rather than diffusing across the depletion region into the
n-layer. Consequently, the hole supply into the epitaxial layer
from the p$^+$ side of the p$^+$-n junction ceases. As a result the
oxide-silicon layer ceases to be inverted, and the device enters the
high impedance state.
(b) Avalanche operation

If the avalanche voltage $V_a$ for the epitaxial n-layer is less than the punch-through voltage, as occurs in relatively highly doped samples ($> 10^{16} \text{ cm}^{-3}$), then the switching voltage becomes a function of the doping density only, as shown in figure 5.11.

For low voltages, a depletion region grows below the gate electrode, as in the case of the punch-through mechanism, but as the voltage across the device approaches $V_a$, the current would increase without limit were it not for the load resistor $R_l$ which limits the current flowing in the circuit. The rapid rise in current initiates the switching action, because when $V_d = V_a$ the large electron current originating in the depletion region is forced across the $p^+\text{-}n$ junction (see figure 5.11(b)). The electron current causes the $p^+\text{-}n$ junction to become forward biased thereby causing positive feedback of holes from the $p^+$ region back into the epitaxial layer. The switching process is now under way, with the hole current inverting the surface of the epitaxial layer (figure 5.11(c)).

The switching voltage $V_s$ is reached when the applied voltage approaches $V_a (12,13)$:

$$V_s = V_a = 60 \left( \frac{\Delta q}{1.1} \right)^{3/2} \left( \frac{N_D}{10^{16}} \right)^{-3/4}$$

(5.3)

It is also observed that breakdown voltages (switching voltage) of the doped layer decrease with increasing doping concentration, and that the switching voltages are considerably less than the
Figure 5.11 Energy band diagrams for the avalanche-mode HISS device:
(a) at low voltages (high impedance);
(b) during switching process;
(c) in low-impedance ON-state(12).
corresponding punch-through voltages for the lightly doped layers.

§5.3.2 Regenerative switching model

Yamamoto and Norimoto(2) have suggested the possibility of a regenerative mechanism of switching related to the build-up of an inverted region in the silicon at the Si-SiO₂ interface. They discovered that in the process of threshold switching, a negative resistance region occurs. The negative resistance can also be observed in devices with the n⁺-p-i-ᵦ configuration and in devices with an n-GaAs substrate used in place of the silicon epitaxial wafer. These results strongly suggest that the negative resistance phenomenon is not limited to the Si-SiO₂ system, but may be observed in different configurations and with various materials.

According to Yamamoto and Norimoto, the mechanism of the negative resistance phenomenon has not yet been clarified completely. They suggested however that one possible explanation involves current multiplication in the MIS structure. Shewchun et al have studied the transport properties in MIS tunnel contacts; their results have appeared in a series of papers(19-23) and they reported a current multiplication process in majority carrier MIS tunnel diodes. The mechanism of the multiplication process in such diodes may be summarised as follows(22):

(a) The degree of inversion at the semiconductor surface under reverse bias can be controlled by the supply of minority
carriers to the surface.

(b) The electric field at the semiconductor surface is strongly dependent upon the degree of inversion at the semiconductor surface.

(c) The majority carrier tunnel current depends strongly upon the potential drop across the insulator and hence upon the surface field. This mechanism results in current multiplication by a factor of 100 to 1000.

When the p-substrate in an MIS device is positively biased the applied voltage is mainly supported by the n-i-n combination, and especially by the depletion region in the n-layer. In this condition, the n-i-n part of the MIS device and an MIS tunnel diode are in the same situation with regard to the process of carrier multiplication which can occur under a suitable applied field and injection conditions. If the bias voltage attains the value at which these conditions are satisfied, holes injected into the n-i-n interface cause the multiplication of current as mentioned above, and a large density of electrons is injected from the metal to the n-layer by tunnelling through the insulating layer. As a consequence, the voltage across the n-depletion region starts to decrease which in turn increases the voltage across the p-n junction, resulting in additional hole injection to the n-i-n part to cause further multiplication of current. This positive feedback continues until a steady state is reached, in which the I-V characteristics resemble those of a forward biased p-n junction.
Yamamoto and Norimoto explain that the sustaining voltage ($V_H$) is slightly larger than predicted due to an additional small voltage drop across the insulator and the n-layer required to maintain the majority tunnel current.

Yamamoto and Norimoto pointed out that although the behaviour of three terminal and coupled devices (see §5.2.1 and 5.2.8) can be consistently explained using the above mechanism, the fact that negative resistance is obtained with various metals, such as Pt, Au, Ni and Al makes the problem somewhat complicated because only Al among these metals is known to have suitable properties for majority carrier MIS tunnel diodes (19). Moreover, a limited range of current levels for carrier multiplication is reported (22). Further, the effect of interface states (24-26) or problems such as thermal diffusion of metal into $SiO_2$ and chemical reaction between them are also considered to affect the phenomenon (25).

Basically the same arguments have been used by Kroger and Wegener (7,8,15) but they present a more detailed model supported by substantial experimental observations. They showed that the choice of insulator material can affect the temperature dependence of $V_s$, as discussed in §5.2.2. A partial explanation of this behaviour involves the different temperature dependence of conduction across the p-n junction and the $Ni-i-n$ interface. The minority current injected by the p-n junction will have a temperature dependence of the form $\exp[-q(E_g-V)/kT]$ where $E_g$ is the silicon bandgap voltage and $V$ is the forward bias voltage. Kroger and Wegener consider, in
particular, the example of a device with a silicon rich nitride i-layer. In this case the insulating layer has been found to have a relationship between current $I$ and voltage $V$ of the form (7)

$$I = I_0 \left\{ \left( \frac{q}{kT} \right)^{\Phi t + \alpha V} \right\}^{1/3}$$

(5.4)

where $I_0$ and $\alpha$ are material constants and $\Phi t$ is a trap or barrier height. The effect of this different temperature dependence on the properties of MISS devices can be pictured as followed.

Suppose the device is biased just below $V_s$. In such a situation minority carriers are injected into the silicon-insulator interface at a rate which is just insufficient to permit a strong inversion layer to form but if the temperature is increased, an inversion layer can form even though the voltage is not increased, because the temperature dependence of the junction conductivity is greater than that of the insulator ($E_g > \Phi t$). Thus even though the insulator can pass more current at a higher temperature, an inversion layer will form (causing the creation of the low impedance state) because the junction will inject minority carriers toward the insulator at an even higher rate. This explanation of the temperature dependence of $V_s$ is, however, incomplete because the relations expressed by equation (5.4) were measured under conditions of accumulation rather than depletion and inversion, and therefore do not necessarily express the conduction across the insulator of the majority and minority carriers of the n-region individually (7). The explanation therefore admits neither the possibility of a generalised
multiplication at the insulator-semiconductor interface (as described by Green and Shewchun(21) for thin SiO₂ layers which conduct by tunneling) nor the rapid change in the ratio of electron-to-hole currents as an incipient inversion layer develops. The latter possibility could occur because of a change in the population of interface states with inversion.

The effect of the injecting p⁺-contact has been illustrated in §5.2.4. By contrast, the temperature variation of Vₛ of a PtSi emitter (Schottky) device is significantly smaller than that of a device with a p-n junction as the emitter. This behaviour is generally observed for Schottky barrier emitters. Consider, for example, the two devices A and C in figure 5.5. Since the ratio of electron and hole currents crossing the Schottky barrier(C) will differ from that of a p⁺-n junction(A)(12,27), so a different distribution of voltage between the collector depletion region and the emitter junction or barrier will be obtained at the threshold voltage condition of the two silicon oxynitride devices. The component of hole current Iₚ crossing the device may be expected to have a dependence on temperature and voltage across the barrier expressed by(28)

\[ Iₚ = A_p^* T^2 \exp\left[\frac{-q}{kT}\left(\Phi_p + V_B - V\right)\right] \]  (5.5)

where A_p^* is the effective Richardson constant for holes, \( \Phi_p \) is the barrier height for holes emitted from the metal into the silicon and V_B is the build-in barrier voltage. Since \( \Phi_p = 0.2V \) for a PtSi-Si
barrier and $V_b = 0.8V$, it may be expected that the temperature
dependence of the PtSi emitter will be less than that of junction
emitter where $E_g = 1.15V$, in agreement with data of figure 5.5.

Adan and Zolomy regarded the switching phenomenon as a
consequence of charge storage effects. The stored charge
accumulated during the ON-state is composed of two parts: a narrow
inversion charge layer at the insulator-semiconductor interface and
a diffusion charge extending from the junction to the interface,
which occupies practically the whole n-layer thickness. After the
device has been turned off the hole inversion and diffusion charge
do not disappear instantaneously, and it takes a certain relaxation
time ($t_0$) for the system to return to equilibrium. The charge
distribution will decay according to a relaxation process given
approximately by

$$\bar{p} = \rho \exp\left(-\frac{t}{t_0}\right)$$

(5.6)

where $\rho$ is a constant, $t_0$ the hole lifetime, and $\bar{p}$ the average
concentration of the holes.

The external voltage across the NiSS diode will rise again when
a time, $t$, after turn-off has elapsed and a depletion layer starts
to be formed. The holes in that part of the n-layer which ultimately
becomes the depletion layer move towards the interface, creating an
inversion layer. After a depletion layer of critical width $d$ has
been established, the threshold field strength in the insulator $E_{th}$
can be calculated as

\[ \varepsilon_0 \varepsilon_i E_{th} = q N_D d + q \tilde{p}(t) d \]  

(5.7)

where \( N_D \) is the donor concentration of the n-layer and \( E_{th} \) the threshold field strength in the insulator, which in fact corresponds to that required to initiate the turn-on process.

In equation (5.7) the inversion charge due to holes injected from the emitter junction is ignored. The threshold voltage \( V_s \) is given approximately by

\[ V_s = \frac{1}{2} \frac{qN_d d^2}{\varepsilon_0 \varepsilon_{si}} \]  

(5.8)

From equations (5.6), (5.7) and (5.8) the threshold voltage may be obtained in the form

\[ V_s = \frac{1}{2} \frac{qN_d}{\varepsilon_{si}} \left( \frac{\varepsilon_0 \varepsilon_i E_{th}^2}{(qN_d + qk \exp(-t/t_0))^2} \right) \]  

(5.9)

or, more simply,

\[ V_s = \frac{A}{(1 + B \exp(-t/t_0))^2} \]  

(5.10)

The results described in §5.2.7 and the calculated values using equation (5.10) are shown in figure 5.12, using the following experimentally determined parameters: \( t_0 = 0.5 \mu s \), \( B = 10 \), \( A = 15.27 \). The calculated values are in reasonable agreement with the experimental

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Figure 5.12 Experimental and Calculated threshold voltage lowering in MISS structures due to charge storage effects. O experimental, Δ theory(18).
results, but are slightly higher probably because in this approximate theory the inversion charge due to injected minority carriers is ignored.

§5.4 Switching in amorphous silicon MIS devices

As mentioned in §4.2.3, Owen et al(29) were the first to report memory switching in GD deposited a-Si:H. In its simplest form the device takes the form of a p⁺-n-i structure where the p⁺- and n-layers are doped from the gas phase, and the i-layer is undoped. Initial structures were made by a-Si:H deposition in the sequence p⁺-n-i onto a stainless steel substrate, followed by the evaporation of Al, NiCr or Au dots (1-2mm in diameter) which form the top contact (see Chapter 6).

It was found that forming was required before the device would exhibit a non-volatile memory switching. Figure 5.13 illustrates this process for a typical p⁺-n-i structure. Curves a and b in figure 5.13 show the unformed (virgin) static I-V characteristics in the forward (p⁺ positive) and reverse (p⁺ negative) directions respectively. When the applied forward potential is increased to 20-25V, a rapid rise in current occurs and the device switches into a highly conducting formed state. The electrical properties of the specimen have been permanently modified by this forming process.

Figure 5.14 shows a typical switching cycle for the GD deposited a-Si:H memory device. Immediately after forming, the
Figure 5.13 Initial static current-voltage (I-V) characteristics in forward direction (curve A) and in reverse direction (curve B) (29).
Figure 5.14 Complete static current-voltage characteristics for forward $p'-n-i$ a-Si:H device, showing forward and reverse threshold voltages, $V_{THF}$ and $V_{THR}$ respectively (29).
device is in the ON-state, and small positive and negative voltages trace out curve ab; an ON-state current of 10 mA or more can be passed through the device. On increasing the reverse potential, a potential \( V_{\text{THR}} \) is reached, beyond which the device switches back to an OFF-state with a resistance of the order of 1 M\( \Omega \), represented in figure 5.14 by the characteristic \( CD \). If the forward potential is then increased beyond a value \( V_{\text{THF}} \), the forward threshold voltage, the device switches back into high-conductivity state ab, in some cases through an intermediate state such as e or f.

In the early experiments (29) the above cycle was repeated up to \( 10^5 \) times without observable changes in characteristics or threshold voltages. The influence of temperature on \( V_{\text{THR}} \) and \( V_{\text{THF}} \) indicate only small changes in either threshold voltage with temperature (e.g. in a particular experiment, \( V_{\text{THF}} \) varied from \(-4V\) at room temperature to \(-3V\) at 450K). The threshold voltages are also unaffected by illumination from filament lamps.

The dynamic responses of a typical \( p^+-n-i \) a-Si:H switch through the OFF to ON and ON to OFF transition are illustrated in figure 5.15(a) and (b) respectively. The transitions were brought about by 10V, 100ns pulses of appropriate polarity superimposed on a 1V pulse of approximately 0.5 \( \mu \)s duration. The purpose of the 1V pulse was to 'read' the state of the switch; it was not a holding pulse to maintain the ON-state. A particular notable feature is that, for both switching transients, the device current responds essentially instantaneously to the voltage signal, i.e. on the time scale of
Figure 5.15 Dynamic switching characteristics of p'-n-i a-Si:H device, using 10V, 100ns pulse superimposed on 1V, ~0.5μs pulse (drawn from oscilloscope traces).
(a) OFF to ON transition (p-layer positively biased);
(b) ON to OFF transition (p-layer negatively biased)(29).
these experiments, at least, there is no delay time involved in the response of the switch. It is estimated that the energy absorbed during either transition is typically in the range $10^{-6}$ to $10^{-8}$ joule\(^{(29)}\).

Gangopadhyay et al\(^{(30)}\) also observed polar memory switching but in hydrogenated sputtered a-Si:H structures in a p\(^{+}\)-n-i sandwich configuration. Figures 5.16(a) and (b) show the virgin static current-voltage (I-V) characteristics of a typical device, with an Al contact to the i-layer, in the forward (p\(^{+}\) positive) and reverse (p\(^{+}\) negative) directions respectively. They found that when the voltage in the forward direction was increased to a certain value (about 9V for a 0.5\(\mu\)m thick device), there was a rapid increase in current and the device switched to a very low resistance ON-state. Figure 5.17 illustrates one switching cycle in the sputtered a-Si:H device.

Gangopadhyay et al\(^{(30)}\) suggested that the ON-state in the switching device is due to the formation of an electronic current filament, but they did not observe any spots on the upper electrode of the device (compare Feldman and Moorjani, §4.1.1). The results of Owen et al\(^{(29)}\) are very similar in most respects to the later observations of Gangopadhyay\(^{(30)}\) on sputtered p\(^{+}\)-n-i a-Si:H memory switches. The only significant differences, so far as one can tell from the published data, is that the sputtered devices have very low ON-state resistance compared to the GD deposited switches (e.g. 2 ohms compared with at least several hundred ohms).
Figure 5.16 Static current-voltage characteristics of a virgin switching device in the forward direction (curve A), in the reverse direction (curve B)(30).
Figure 5.17 Static current-voltage characteristics of a formed p⁺-n-i a-Si memory switching device, showing the ON and the OFF state (30).
References


CHAPTER 6

DEVICE FABRICATION AND EXPERIMENTAL TECHNIQUES

§6.1. Device structure

§6.1.1 Basic device configuration

The structure of the amorphous silicon (a-Si:H) memory device in its simplest form is illustrated in figure 6.1. It consists of three layers of a-Si:H, deposited onto a suitable substrate, in the sequence p\(^+\)-, n- and i-type where "i" stands for intrinsic (or undoped) a-Si:H or some other appropriate insulator (see later for example). In some respects two layer p\(^+\)-i and (notionally) p\(^+\)-n structures have similar properties. As will be mentioned in Chapter 7 the a-Si:H layers may also be in the sequence n\(^+\)-p-i (or n\(^+\)-p) and with appropriate changes in polarity of applied voltage, such devices would have equivalent characteristics. Basically similar memory switching has also been reported in a-Si:H devices having a p-i-n configuration but as far as is known they have not been so thoroughly studied(1). All of the work reported in this thesis is concerned with memory switching devices in the p\(^+\)-n-i or p\(^+\)-i configurations.

A variety of materials may be used as the substrate in the simple device structure illustrated in figure 6.1. In some of the
Figure 6.1 A schematic diagram of the a-Si:H memory device ("dot" contact).
early experiments, when relatively large scale devices were being studied, it was convenient to use polished stainless steel plates and in this case the substrate also functions as the bottom electrical contact of the device. More generally, an insulating substrate of Corning 7059 glass is preferable (particularly for the fabrication of small scale devices by microlithographic techniques), and in this case it is necessary to first deposit a thin-film metal contact onto the substrate surface.

The simple device is completed by a disc or "dot" thin film metal top contact deposited through a contact mask. The smallest top contacts which may be conveniently prepared in this way have a diameter of ~0.5mm. A variety of metals may be used as top and bottom contact materials, e.g. Cr, NiCr, Al and they can be deposited either by vacuum (thermal) evaporation or r.f. sputtering.

The total thickness of the three (or two) a-Si:H layers was in the range ~0.1 - 1μm. Individual thicknesses of the layers were varied and will be quoted for specific devices along with doping levels in Chapter 7 with the experimental results.

§6.1.2 "Pore" devices

Early experiments indicated that the "dot" contact devices were less than ideal for the study of switching in a-Si:H p\(^+\)-n-i layers. The primary difficulty was related to the accurate control of device area, which has a bearing on the following:
In its OFF-state, the a-Si:H memory switch has a capacitance proportional to the area of the top contact. The energy stored in the capacitor is discharged through the device at the instant of switching and if that energy (capacitance) is too large it can damage or even destroy the device.

Evidence for or against filamentary conduction could be gained from measurements as a function of contact area.

For practical applications in microelectronics the a-Si:H memory device should be as small as possible (e.g. integrated circuit devices in current production typically have critical dimensions of the order of 2μm).

For these reasons techniques for the fabrication of the a-Si:H memory switches in a "pore" structure were developed; the layout and configuration is shown schematically in figure 6.2. The active area of the device is defined by a circular hole, or "pore", etched into a photoresist layer deposited on top of the a-Si:H layers. Further details of the "pore" structure can be found in §6.2.2.

§6.2 Fabrication

§6.2.1 Deposition of amorphous silicon

In this project the a-Si:H deposition and most other steps in the fabrication process were carried out by Professor U.E. Spear and
Figure 6.2 (a) Plan view of a single a-Si:H memory ("pore") element. The diameter $d$ of the active area is defined as shown.

(b) Cross-section through the element along the line A-A'.

Bottom Contact (Electrode)
his colleagues in the Carnegie Laboratory of Physics at the University of Dundee. Thin films of a-Si:H were prepared by the glow discharge decomposition (GD) of silane and the experimental arrangement is shown schematically in figure 6.3. The gas, G, flows through the quartz reaction tube, T, past the substrate, S, which is held on a heated pedestal, H. The plasma, P, is maintained by inductive coupling (figure 6.3(a)) or capacitive coupling (figure 6.3(b)) of r.f. power into the gas. The power level is typically 10 - 20 watts, and frequencies between 1 and 100 MHz have been used(2).

The electronic properties of GD a-Si:H are critically dependent on variables such as the substrate temperature, flow rate, pressure, r.f. power level, the floating potentials on specimen and other surfaces, the tube diameter and also the position of the coil with respect to the substrate. It has been shown that the structure of the film can be changed drastically by relatively small changes in the substrate temperature and position, but the significant point of using the glow-discharge technique is that the plasma remains in close contact with the specimen surface. In the preparation of a-Si:H from silane, complex surface reactions take place during growth, involving electrons and positive ion fragments such as SiH, SiH₂, SiH₃. The experimental control of these surface reactions to obtain well-defined and reproducible electronic specimens is of utmost importance.

As described in §6.1.1, the a-Si:H memory devices studied in this project are two- or three-layer structures but the most
Figure 6.3 Diagrams illustrating experimental methods for gas-phase deposition of a-semiconductor; (a) inductive coupling of the r.f., (b) capacitive coupling(2).
frequently studied structure is the $p^+\cdot n\cdot i$ configuration. The $p^+$- and $n$-layers of $a$-$Si:H$ are obtained by gas phase doping by adding small but accurately determined amounts of the hydrides of a pentavalent (e.g. phosphine) or trivalent (e.g. diborane) impurity to the silane. A schematic diagram of the preparation unit developed at Dundee is shown in figure 6.4. The silane is mixed with the doping gases in the glass cylinders $C_1$ and $C_2$ respectively. For the preparation of an $n$-type mixture, phosphine is first admitted into a small known volume and its pressure measured with a pressure transducer $P.T.$.. It is then expanded into the evacuated cylinder $C_1$ and silane added to attain a standard pressure. In this way it is possible to add with a reasonable degree of accuracy a few volume parts per million of phosphine to the silane. Similarly, diborane can be pre-mixed in cylinder $C_2$ for doping with a $p$-type impurity. Therefore any desired sequence of $n$- and $p$-type layers can be deposited by opening and closing the appropriate taps. The flow rate is measured by the electronic flow meter, $F$, and decomposition takes place in the $r.f.$ glow-discharge between $A$ and $B$ of the chamber. Due of the toxic nature of the gases used, independent evacuation and nitrogen flushing facilities are incorporated in the apparatus.

§6.2.2 Device fabrication by photolithographic technique

As mentioned in §6.1.2 it was found necessary to establish techniques for the fabrication of small devices for standard microlithography, i.e. "pore" structures. Figure 6.2(a) shows a
Figure 6.4 Schematic diagram of the preparation unit for n- and p-type a-Si specimens developed by the Dundee group. $C_1$, $C_2$, glass cylinder; P.T., pressure transducer; $F$, flowmeter; S, substrate(2).
Plan view of one structure in a 10 x 8 array produced by photolithographic technique, and figure 6.2(b) represents a cross-section through the same structure. Fabrication was carried out by typical microlithographic techniques using in-contact photoresist (PR) masks to produce the pore and contact electrode patterns. The bottom electrode pattern was fabricated first and the substrate placed into the deposition unit and cover with a-Si:H. After etching the a-Si:H squares, of sides 600μm, the sample was coated with photoresist. After etching of the pore the remainder of the resist layer was left in place as an insulator to define the active area (see figure 6.2(b)). The designation "a-Si:H" in figure 6.2 means the appropriate sequence of p⁺-n-i, p⁺-i layers. A number of mask-sets were produced which enabling structures with diameters ranging from 300μm down to about 2μm to be fabricated. These have been used to study the area and temperature dependence of the switching parameters, such as threshold voltages, ON- and OFF-state resistances and switching times, of a series of p⁺-n-i a-Si:H layers.

§6.2.3 Fabrication procedure

The fabrication procedure of the pore structures is as follows:

(1) A Corning 7059 glass slide is degreased with Teepol using a microcloth, rinsed in deionised water, and blown dry with nitrogen.
(2) The bottom electrode metal is deposited and a layer of photoresist (AZ1350H) coated on top of the metal using a spinner (see figure 6.5(a)).

(3) The PR is IR baked for 10 minutes to harden its surface enabling a photolithographic mask to be placed on top of it.

(4) The glass slide with the metal and PR is then exposed to UV light through a photolithographic mask as shown in figure 6.5(b).

(5) The exposed part of the PR is then washed away in AZ developer (see figure 6.5(c)) and rinsed in deionised water.

(6) The glass slide is baked at 130°C for 30 minutes. This is to further harden the PR prior to the metal etch.

(7) The unprotected part of the metal (marked "U" in figure 6.5(d)) is etched away with appropriate etchant.

(8) The hardened PR is removed by dipping in acetone.

(9) Cleaning repeated as outlined in step (1).

(10) GD a-Si:H is deposited.

(11) Deposited a layer of aluminium (Al).

(12) The whole device is coated with PR (see figure 6.5(e)).
Figure 6.5 Schematic diagram of the pore structure fabrication procedure (Not to scale).
(13) Steps (4), (5) and (6) are repeated.

(14) The unprotected portion of Al (marked "U" in figure 6.5(f)) is etched away with appropriate Al etchant.

(15) The a-Si:H is etched using HMT 6:1:1 silicon etch.

(16) Harden PR is removed as in step (8).

(17) The remaining Al is removed.

(18) Cleaning repeated as stated in step (1).

(19) The whole slide is cover with PR.

(20) The pore area is defined as per steps (3), (4) and (5).

(21) The slide is baked at 200°C for 30 minutes to completely harden the PR.

(22) Cleaning repeated as in step (1).

(23) Top metal electrode metal is deposited.

(24) As step (12)

(25) Steps (4), (5) and (6) are repeated.

(26) As steps (7) and (8) and the final pore structure is shown in figure 6.5(g).

The aluminium layer in step (11) is deposited as it was found that when etching a-Si:H, the etchant (HMT 6:1:1 silicon etch) usually etches away the protected a-Si:H if only PR was used as a protective
layer. Cr is usually used as the bottom electrode material as a-Si:H adheres well to Cr. The adhesion to Al is poor because an oxide layer tends to form on top of the Al layer. The etchants used for etching away Al and Cr were HfC aluminium etch and HfC chrome etch respectively.

The individual thicknesses of the $p^+$-, n- and i-layers are estimated from the deposition time for each layer and its deposition rate. The doping level of each layer is measured indirectly by the pressure transducers of the glow discharge unit as depicted in figure 6.4. Although previous work(2) has shown that approximately 30% of the dopant atoms are active, a much lower doping efficiency has been reported recently(3) which suggests that this correlation should be treated with caution. The flow rate of silane is a few c.c. per minute. As is described in Chapter 7, a-Si:H memory devices with SiN replacing the i-layer have also been investigated, and in this case the SiN is obtained by r.f. decomposition of a mixture of silane and ammonia.

§6.3 Experimental techniques

§6.3.1 Current-Voltage (I-V) measurements

Current-Voltage (I-V) measurements were performed as a function of parameters such as temperature, n-layer thickness and doping. The experimental setup used to obtained I-V characteristics is shown in
Figure 6.6. The sample, S, was connected to a power supply capable of supplying at least 25 volts. The voltage drop across the sample was measured by a Gould multimeter and the current by a Keithley electrometer model 610C.

Care needs to be taken in measuring the I-V dependence of the a-Si:H devices as a function of temperature and to explain the reasons it is necessary to anticipate some of the experimental results which are presented in detail in Chapter 7. When a voltage (bias) is first applied, in the forward direction, to a freshly prepared (virgin) device the measured current generally remains constant after any initial capacitive decay. After the lapse of a given time, which depends on the voltage level and temperature however, the current through the device is observed to increase more or less instantaneously to another constant but higher level. The elapsed time is called the delay time \( t_D \) and the corresponding voltage is called the forming voltage \( V_F \).

The forming voltage and \( t_D \) are interrelated and the phenomenon is temperature dependent (as \( V \) increases, \( t_D \) decreases—see Chapter 7 and references (5) and (6)). The term "forming" is used to describe this phenomenon because, subsequently all switching operations occur at a much lower voltage. It is similar to the forming process sometimes observed in crystalline NISS structure (see Chapter 5). The existence of the forming operation means that care has to be taken in measuring initial I-V (or C-V) characteristics.
Figure 6.6 Circuitry used for the investigation of static and dynamic properties. The typical waveforms of voltage ($V_s$) and current flow across the sample ($I_s$) as a result of switching from OFF to ON state are also shown.
Current-voltage characteristics were also measured using a Hewlett-Packatt Semiconductor Parameter Analyser 4145A. This instrument is designed to measure, analyse, and graphically display d.c. parameters and characteristics of diodes, transistors and integrated circuits. For device measurement and simulation, the HP4145A is equipped with four programmable stimulus/measurement units (SUUs). Each SUU can be programmed to function as a voltage source/current monitor (V mode) or a current source/voltage monitor (I mode). Mode changes and channel reassignment are fully automatic, eliminating test lead connection changes. Each SUU can output and measure up to 100mA and 100 V and the measured/applied current or voltage can be as low as 1 pA and 1 mV respectively. With the HP4145A the time taken for each I-V measurement is significantly reduced compared with point-by-point measurements allowing a greater device throughput. The 4145A was connected to a HP microcomputer model 9816A to control the I-V measurements.

§6.3.2 Capacitance-Voltage (C-V) Measurements

Capacitance-voltage measurements were carried out using a Hewlett-Packatt 4280A 1MHz meter/C-V plotter. This instrument is designed to measure the C-V and C-t characteristics of semiconductor devices and materials. The test signal is a 1 MHz sine wave and the measurement terminals are in a "two-terminal pair configuration", which, when properly connected to the device under test eliminates mutual inductance between test leads and reduces the effect of
environment noise. The built-in d.c. bias source has an output capability of 0 to 100 V, with 1 mV setting resolution on the most sensitive range. For C-V measurements the bias voltage can be swept either in a single staircase or double staircase fashion. Initial hold time and step delay time from 3 ms to 650 s can be set to allow the device under test to stabilise at each voltage step before measurement is made(7).

A schematic diagram of the experimental arrangement for the C-V measurements is shown in figure 6.7. The device under test was enclosed in an aluminium box to prevent interference from light or environmental noise. The HP4280A was interfaced with a HP9816A microcomputer which can be used to control the C-V measurement automatically by typing in appropriate maximum and minimum bias and bias step. With this programme, it is also possible to plot out the C-V graphs on a HP plotter (Model 7475A).

§6.3.3 Dynamic (transient) measurements

The forming process, i.e. the first OFF → ON transition, does not occur instantaneously when a voltage step or pulse is applied to the a-Si:H p⁺-n-i device. A delay time ($t_D$) is observed, after which the current begins to increase, rising almost instantaneously to its ON-state value. It will be shown in Chapter 7 that the forming delay time is an extremely sensitive function of the applied forming voltage; it varies over nearly ten orders of magnitude, from a few hundred seconds at low forming voltages to about 10 ns at high
Figure 6.7 Circuitry used for the capacitance-voltage (C-V) measurement.
In order to measure the delay time, it is firstly necessary to consider its order of magnitude. For delay times larger than several seconds the d.c. measurement techniques described in the previous section can be used. However, when the applied voltage is larger, the delay time is in the microseconds to nanoseconds range and therefore single pulse experiments must be used to obtain accurately the delay time and the forming voltage and current. The experimental apparatus for these fast transient measurements is shown in figure 6.6. The voltage drop across the device was measured using a Tektronix Storage Scope (Model 7633). The current passing through the device was deduced from the voltage drop across the resistor $R_2$. The load resistor $R_L$ is employed in this fast transient measurement to prevent the device switching to a very low resistance ON-state, by limiting the current passing through the device after forming.

The current instabilities mentioned in §7.2.6 were measured as follows. Pulse measurements were taken primarily using a Hewlett-Packard pulse generator (Model 8160A) source; with the voltage and current being displayed on a digital storage oscilloscope (Model HP54200A). In cases where a long delay (>100μs) between consecutive short voltage pulses was required, an additional pulse generator was used as a trigger source and a Tektronix oscilloscope (Model 7633) used to monitor the current corresponding to the second pulse. The trigger signal for this instrument was conditioned using a divide by
two circuit, and time between pulses determined using an interval timer. Measurements at temperatures other than ambient were taken with the sample mounted on a metal block held at an appropriate temperature, under vacuum if necessary to avoid water condensation.

§6.3.4 Other techniques

In Chapter 7 the results of the I-V, C-V and transient measurements on the a-Si:H memory devices form the bulk of the experimental results. Other experiments, such as the observation of the ON-state filament using liquid crystal(8), and the scanning electron microscope (SEM) work on the pore structure will also be reported. The experimental setup for these measurements, will be described at the appropriate points in Chapter 7.
References


The fabrication of a-Si:H memory devices was discussed in Chapter 6, and several device configurations have been investigated in this work. Before reporting the results, it is useful to look at the basic switching operation of the formed memory device(1). A typical set of static d.c. characteristics of a formed device, measured on a curve tracer, is shown in figure 7.1. The upper right quadrant corresponds to a positive bias on the p⁺-layer of the p⁺-n-i structure and this will be referred to as the FORWARD direction. Immediately after forming (see below), the device is in an ON-state so that small positive and negative voltages trace out curve ab; ON-state currents of up to 10mA are generally observed. On increasing the reverse potential, a reverse threshold voltage $V_{THR}$ is reached, beyond which the device switches to an OFF-state with a resistance of the order of $1\Omega$, represented in figure 7.1 by the characteristic cd. If the forward potential is then increased beyond a value of $V_{THF}$, the forward threshold voltage, the device switches back to its high conductivity state ab, in some cases through an intermediate state such as e or f.

For all of the configurations investigated it was found that before the device can function as a non-volatile switch, a first switching operation, i.e. a forming process, is needed. This
Figure 7.1 Complete static current-voltage characteristics of a formed a-Si:H p'-n-i device, showing the forward (i.e. positive voltage applied to the p'-region) and reverse (i.e. negative voltage applied to the p'-contact) threshold voltages $V_{THF}$ and $V_{THR}$, respectively.
forming is unique; all following cycles occur, reproducibly, at a considerably lower threshold voltage. Figure 7.2 illustrates the forming process for a typical p'-n-i structure. In this case all the measurements were taken point-by-point and can be considered as true d.c. measurements. Curve A in figure 7.2(a) is the initial static I-V characteristic in the forward direction. Curve B represents the initial reverse characteristic. When the applied forward potential is increased to a certain value which is determined by the device geometry and temperature etc, a rapid rise in current takes place and the device is brought into a highly conducting formed state, represented by curve C in figure 7.2(b). The electrical properties of the device have been permanently modified by this forming procedure. The newly prepared device which has not been through the forming process is thus called the virgin device.

Although this work is concerned mainly with the forming process in non-volatile a-Si:H memory devices, it is inevitable that the electrical properties of the virgin devices and, to a somewhat lesser extent the ON- and OFF-states, should also be considered in order to provide a more comprehensive account of the forming process. The results obtained in this work are thus divided into three main sections, namely the virgin state, the forming process and the formed device, i.e. the ON- and OFF-states.
§7.1 The virgin state

The I-V characteristics of virgin a-Si:H p⁺-n-i structures are determined by many device parameters, such as the thickness of the n-layer (dₙ), the metal contact made to the i-layer and temperature. To describe the static I-V characteristics of the virgin devices systematically, several subsections which emphasise the role of particular device parameters are presented. Most of the results obtained in this work relate to p⁺-n-i structures and the most thoroughly studied parameter is the role of the n-layer (for reasons to be explained in Chapter 8). Nevertheless, static I-V measurements were also made on other device structures such as p⁺-i, p⁺-n-v (v : lightly n-doped) structures etc.

§7.1.1 Temperature dependence of I-V characteristics

The forward bias static d.c. characteristic shown in figure 7.2(a) also depicts the forming process of a-Si:H p⁺-n-i structures at room temperature. In the forward bias direction there is a region of ohmic behaviour at low voltages, followed by a region where $I \propto V^2$ (marked P in figure 7.2(a)) and at higher applied voltages $I \propto V^m$ (i.e. region H in figure 7.2(a)) where $m > 2$. To emphasise the non-ohmic behaviour, figure 7.3 depicts typical I-V characteristics, on a linear scale, at three temperatures. The onset of the highly non-ohmic region is marked by the arrow. At this point the device begins to become unstable and it is impossible to continue with point-by-point measurements.
Figure 7.2 (a) Initial static current-voltage characteristics of a virgin a-Si:H p+-n-i structure in forward direction (Curve A) and in reverse direction (Curve B).
(b) I-V characteristic in formed conducting state (Curve C).
Figure 7.3 Typical I-V characteristics for a-Si:H p⁺-n-i device (xSi262) with different temperatures as stated in the diagram.
As the ambient temperature increases, the onset of non-ohmic behaviour moves to lower voltages. In the reverse direction, there is also an initial ohmic region but the change to non-ohmic behaviour in this case is much more gradual, leading to the eventual breakdown of the device. It can also be seen from figure 7.3 that the reverse current is less sensitive to variation in temperature compared with the forward current.

§7.1.2 I-V characteristics with different n-layer thicknesses

It was found that the current density versus voltage (J-V) characteristics of virgin a-Si:H p⁺-n-i structures depend on the n-layer thickness \(d_n\). Four samples (ASi33, xSi513, xSi316, and J169Y) † were used to study this dependence. One sample (J169Y) is a p⁺-i structure (i.e. n-layer thickness is zero). The sample parameters are given in Table 7.1 and the forward and reverse bias J-V characteristics are shown in figures 7.4 and 7.5 respectively. Current density (J) is plotted in these figures in order to compare devices of different area, and this representation will be used in the following sections where samples of different area are to be compared.

It is interesting to note that the forward bias J-V curves of the four samples behave differently when the n-layer thickness is less than a critical value \(d_{nCR}\). Sample ASi33, with an n-layer thickness

† The sample notation adopted by the Dundee group is used throughout this thesis.
<table>
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<th>Sample No.</th>
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<th>Deposition (data)</th>
<th>Deposition (min.)</th>
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<th>Total Thickness (mm)</th>
<th>Substrate</th>
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<td>0.24</td>
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SS : Stainless Steel
T₀ : Substrate temperature

Table 7.1 Details of samples used in this work.
Figure 7.4 The forward J-V curves of virgin a-Si:H p\textsuperscript{+}-n-i devices with different n-layer thicknesses.
Figure 7.5 The reverse J-V curves of virgin a-Si:H p⁺-n-i devices with different n-layer thicknesses (sample details see Table 7.1).
thickness of 300nm, has a J-V dependence very similar to the p⁺-i structure (J169Y) while the J-V characteristics of samples xSi543 and xSi316 are entirely different.

The forward bias J-V characteristics of p⁺-n-i structures with \( d_n < d_{nCR} \) resemble those of the p⁺-i structure, while with \( d_n > d_{nCR} \) there is a regime where \( J \propto V^2 \) (marked P in figure 7.4) which is not found in devices with \( d_n < d_{nCR} \). Hence the region where \( J \propto V^2 \) seems to be associated with the n-layer and will only manifest itself clearly when \( d_n > d_{nCR} \). It can also be seen from figure 7.4 that the highly non-ohmic region occurs at lower voltages as a result of decreasing the n-layer thickness (this is similar to the effect of changing the ambient temperature - see §7.1.1). In contrast, the reverse bias J-V curves are relatively insensitive to changes of the n-layer thickness as shown in figure 7.5. In Chapter 8 the results shown in figure 7.4 will be analysed in detail.

§7.1.3 I-V characteristics with different n-layer doping

Four samples (ASi58, ASi93, ASi94 and xSi316) were used to investigate the effect of n-layer doping, and the results are shown in figure 7.6. Note that ASi58 and xSi316 both have an n-layer doping level of 30 vppm while in ASi93 and ASi94 the level is 202 vppm (see insert of figure 7.6).

Notice first of all that if samples with the same doping levels are compared (i.e. ASi58 and xSi316; or ASi93 and ASi94), the
Figure 7.6 The forward bias J-V characteristics of a-Si:H virgin devices with different n-layer doping.
variation with n-layer thickness is in accord with observations described in §7.1.2. Moreover, the J-V characteristic of sample ASi58, which has a rather thin n-layer (~200nm), resembles the characteristic of a p⁺-i sample, again as noted in §7.1.2.

On the other hand, in the case of ASi94, which has a relatively thick, heavily doped n-layer, the J-V characteristic falls in between those of the two lightly doped samples (ASi58 and xSi316). Thus, increasing the doping level moves the J-V characteristics in a way equivalent to an increase of $d_{nCR}$. Finally, for sample ASi93 which is heavily doped (the same as ASi94) but has a thin n-layer, the characteristic is similar to ASi58 (i.e. like a p⁺-i sample). This is probably because if the n-layer is relatively thin the doping level will have little effect, however large it might be.

Thus, it seems that $d_{nCR}$ increases as the n-layer doping level increases. Another feature apparent in figure 7.6 is that the voltage at which the current rises very steeply is also reduced as the n-layer doping is increased (indicated by the arrows).

§7.1.4 I-V characteristics with different top metal ($M_1$) contacts

To investigate the role of the metal contact ($M_1$) to the i-layer of the p⁺-n-i structure, three samples designated ASi156 were prepared, one with aluminium(Al), another with titanium(Ti) and the third with chromium(Cr) as the contact $M_1$. Typical J-V characteristics of identical p⁺-n-i structures with different metal
contacts are shown in figure 7.7.

When forward biased, there is a marked difference in the J-V characteristics, depending on the $\text{M}_1$-i contact, as shown in figure 7.7(a). At a fixed bias, devices with a Ti top contact are the most conducting while Al devices are the least conducting and at voltages $\geq 1\text{V}$ the difference is nearly six orders of magnitude. In the reverse bias direction the nature of the metal has only a small influence on the J-V characteristics (figure 7.7(b)).

It should be noted that the $p^+-n$ junction is identical in all three cases and hence the different J-V dependence can only be attributed to the $\text{M}_1$-i junction. The $\text{M}_1$-i interface would be expected to behave as a Schottky barrier which is reverse biased when the $p^+-n$ junction is forward biased and vice-versa. The $\text{M}_1$-i interface seems less blocking to holes when the metal is Ti or Cr. It is also worth noting that the n-layer in A5i156 is thinner than usual (44nm), and is perhaps commensurate with the $p^+-n$ depletion width.

§7.1.5 Area dependence

Using photolithographic techniques a series of unformed "pore-type" $p^+-n$-i specimens were prepared with the pore ranging in diameter from 5μm to 300μm (see §6.2.2 and 6.2.3). The area dependence of the virgin state forward bias resistance $R_u$ of this series of samples is shown in figure 7.8. The values of $R_u$ were
Figure 7.7 Static J-V characteristics for the a-Si:H devices (ASi156) with different top metal contact as stated. (a) forward bias; (b) reverse biased.
Figure 7.8 Virgin state resistance $R_u$, measured at 0.5V, of $p^+\cdot n\cdot i$ structures (A5i82) plotted as a function of their area $A$. 
calculated from the ratio of voltage to current at an applied forward voltage of 0.5V. Although there is some scatter in the data, probably caused by variations in area during processing, the data follow the behaviour expected from simple geometrical factors, viz: \( R_u = A^{-1} \), as shown by the full line. This result demonstrates that in the virgin state the current flows uniformly throughout the area of the specimen.

§7.1.6 Capacitance-Voltage (C-V) Measurements

C-V measurements at 1Hz were carried out on virgin devices (J169Y, xSi403 and xSi265) with different n-layer thicknesses. The experimental arrangement is described in §6.3.2. An Al top contact was used in all these samples and the C-V plots are depicted in figures 7.9, 7.10 and 7.11.

As described in §7.1.2 the J-V characteristics of a-Si:H p+-n-i devices depends on the n-layer thickness. It is found that the C-V characteristics exhibit a similar dependence. From figures 7.9 - 7.11, it can be seen that as the n-layer thickness is reduced from 660nm to zero (i.e. p+-i), the C-V characteristics change substantially. The C-V characteristics of J169Y and xSi403 are similar, and it is interesting to note that figure 7.9 (J169Y) resembles the C-V plot of an MOS capacitor. The C-V plots of devices with thicker n-layers (>400nm) have a peak slightly below zero bias. The C-V characteristics of c-WISS devices (see (2) and §5.2.3) are similar to figure 7.9 (i.e. devices with the thicker n-layers), and
Figure 7.9 Capacitance-Voltage (C-V) plot at 1MHz for virgin a-Si:H p'-i structure (Sample J169Y).
Figure 7.10 C-V plot at 1MHz for virgin a-Si:H p⁺-n-i structure (Sample xSi403, d_n=215nm).
Figure 7.11 C-V plot at 1MHz for virgin a-Si:H p⁺-n-i structure (Sample xSi265, dᵣ = 660nm).
The results in previous sections on the J-V characteristic of a-Si:H memory devices were taken either by point-by-point methods or using the HP4150A Semiconductor Parameter Analyser. Under forward bias and at room temperature, the a-Si:H p⁺-n-i devices tend to become unstable at higher bias, depending on the thickness of the sample and other device parameters. At higher temperatures the onset of instability occurs at lower voltages, as indicated by the arrows in figure 7.3. On attempting to increase the voltage still further the device switches spontaneously into a low-resistance ON-state. The device can now be used as a switch as outlined in §7.1. All subsequent operations occur at a much lower voltage than the first, e.g. at ~5V for the WRITE operation compared with the first switching operation (forming) at ~25V observed under the conditions obtaining for the measurements shown in figures 7.1 and 7.2(a).

The circuitry used to study the dynamics of the forming process has been discussed in §6.3.3. The forming process, i.e. the first OFF to ON transition does not occur instantaneously when a voltage
step or pulse is applied to the device (see §6.3.1 and 6.3.3). Initially there is a delay time $t_D$, during which the device current remains essentially constant at the virgin-state value appropriate to the voltage across the device. Only after this delay does the current begin to increase and it then rises essentially instantaneously to its ON-state value.

The forming delay time is an extremely sensitive function of the applied voltage and typical data, obtained at three temperatures, are illustrated in figure 7.12. The delay time varies over nearly ten orders of magnitude from a few hundred seconds at low forming voltages to about 10 nanoseconds at high voltages. In particular, at a temperature-dependent critical voltage $V_{CR}$ there is virtually a discontinuous change in $t_D$ as a function of bias(3,4). The voltages $V_{CR}$ indicated in figure 7.12 are roughly coincident with the voltages at the points of instability marked by the arrows in figure 7.3. The voltage $V_{CR}$ also corresponds approximately to the forming voltage which would be obtained in an experiment on a virgin device with a curve tracer. Note in figure 7.12 that above and below $V_{CR}$ the delay time tends to a value which seems to be approximately independent of both voltage and temperature; for the particular results illustrated $t_D$ is in the range $10^2$-$10^3$ seconds for $V < V_{CR}$ and in the range 10-100 nanoseconds for $V > V_{CR}$.
Figure 7.12 The delay time \( t_D \) for forming of a typical a-Si:H p'-n-i structure (xSi262) as a function of applied voltage at three different temperatures: (0) 30°C, (o) 80°C, (+) 160°C.
§7.2.3 Forming with different n-layer thicknesses

For this experiment, eight samples (AS133, AS158, xSi304, xSi316, xSi401, xSi543, xSi547 and xSi549) having i- and p⁺-layers as similar as possible were chosen. The circuitry used to study the forming process with different n-layer thicknesses was the same as in §7.2.2. It was found that the forming voltage ($V_F$) increases linearly with the thickness of the n-layer where $d_n > d_{nCR}$ and typical data are shown in figure 7.13 (for all these samples the doping level is 30 vppm and from previous results, therefore, $d_{nCR}$ would be ~350nm). The forming voltage $V_F$ is recorded by applying a minimum voltage pulse so that the device is formed. It is found that $V_F$ coincides approximately with the voltage $V_{CR}$ indicated in figure 7.12. Note that for $d_n > d_{nCR}$, the results do not extrapolate to zero n-layer thickness but it can be seen from figure 7.13 that when $d_n < d_{nCR}$, the $V_F$ versus $d_n$ plot falls below the extrapolation from $d_n > d_{nCR}$. The possible implications of this finding are discussed in Chapter 8.

§7.2.4 Forming with different i-layer thicknesses and contact areas

In these experiments three a-Si:H p⁺-n-i devices (ASi80, ASi81 and ASi99) were formed using a fast rising voltage pulse of about 350 nanoseconds duration. It was found that $V_F$ slowly increases, by about a factor of three, as the area of the specimen decreases by about three orders of magnitude as shown in figure 7.14.
Figure 7.13 Illustration of the variation of the forming voltage, $V_F$, on applying a voltage pulse, with the thickness of the $n$-layer. In all the samples, the $n$-layer doping level is 30 vppm.
Figure 7.14 The area dependence of the forming voltage, $V_F$, for three $p^+\text{-}n\text{-}i$ structures with the i-layer thickness $d_i$, as shown.
For a particular contact area (e.g. $10^{-6} \text{cm}^2$) the results in figure 7.14 show that as the i-layer thickness ($d_i$) is reduced from 42nm to 9nm, $V_F$ decreases from 26V to 20V. The decrease in $V_F$ is not proportional to $d_i$ as one might expect if the forming process is purely field dependent. Actually, according to a model to be presented in Chapter 8, the precise field distribution across the i-layer is unlikely to scale with the applied voltages or to be inversely proportional to i-layer thickness.

§7.2.5 Forming with different $M_i$-i metal contacts

The static and pulsed I-V characteristics of devices ASi153 and ASi162 with Cr $M_i$-i contacts exhibit certain properties which contrast with devices with Al contacts such as ASi81 and ASi82 (see also §7.1.4). The latter are referred to in the following as type A and the former as type B devices.

Type B devices form at similar voltages to type A (15 to 25V) but do not necessarily form to a low resistance state ($<10k\Omega$) directly. They sometimes form into a typical OFF-state ($10^5$-$10^6 \Omega$ measured at 1V) with non-linear I-V characteristics. Repeating the forming pulse usually completes the forming to a lower resistance state (1 to 10kΩ) which is slightly non-linear but reasonably symmetric, as depicted in figure 7.15. Type A devices almost always form directly to a low resistance ($10^2$-$10^3 \Omega$) state and have a linear, symmetric I-V characteristic in this state (more detail on the ON-state will be given in §7.3.1). However, during the course
Figure 7.15 The I-V dependence of type B device (ASi162) at various resistance states.
of this work, it was discovered that sometimes type A devices can be formed into an "intermediate" state. When the device (Asi94) is formed into an intermediate state, it acts as a threshold switch (5). The switching operation of this threshold switch is illustrated in figure 7.16. When the applied bias exceeds a threshold, $V_{TH}$, the device switches instantaneously into a higher conducting state ("H" in figure 7.16), and if the voltage is reduced below $V_{TH}$ the device reverts to the lower conducting state (L in figure 7.16). It is worth noting that Asi94 has an n-layer doping level (202 vppm) higher than that normally used.

It is also found that type B devices do not appear to have two distinct intrinsic resistance states (cf. $10^2$-$10^3 \Omega$ for $R_{ON}$ and $> 10^7 \Omega$ for $R_{OFF}$ for type A devices). Typical type B devices have a band of $R_{ON}$ from 1 to $10k\Omega$, and $R_{OFF}$ from $10k\Omega$ to $1M\Omega$. However when the device is working properly (i.e. cycling through ON- and OFF-states for at least $10^3$ times) a separation of $R_{ON}$ and $R_{OFF}$ of 2 to 3 orders of magnitude can be maintained.

§7.2.6 Current instabilities in virgin devices

Current instability phenomena have been observed at voltages below those required for forming in virgin a-Si:H $p^+\text{-}n\text{-}i$ structures in which the i-layer is significantly thinner than that normally used (<10nm, see Table 7.1)(6). The principal features associated with the current instabilities are shown in figure 7.17. A voltage pulse $V$, greater than a minimum threshold $V_{C}$, is applied such that
Figure 7.16 Threshold switching of formed "intermediate state" a-Si:H p⁺-n-i structure (ASi94).
Figure 7.17 A schematic illustration of the various parameters in the transient current instability in virgin a-Si:H p-n-i device with thin i-layer (~10nm).
the $p^+$-layer is positively biased. A displacement current occurs which decays quickly to a steady current $I_s$. Some time $t_{on}$ after the voltage pulse has been applied the current rises abruptly, with a characteristic rise time $\tau_r$. After reaching a maximum value $I_{max}$ the current decays with a characteristic fall time $\tau_f$. A second voltage pulse is applied at a time $t_r$ after the first. This may or may not give rise to a current instability depending upon the values of $V$ and $t_r$.

The dependence of the onset time $t_{on}$ on pulse height $V$ and temperature $T$ for a typical sample is shown in figure 7.18. It can be seen that onset times in the range 0.3 to 10$\mu$s show an exponential dependence on $V$ of the following empirical form:

$$t_{on} = t_{ono} + t_o \exp \left[ \frac{-(V-V_C)}{V_o} \right]$$

(7.1)

where $V_o$ is usually in the range 0.6 to 0.8V and, for a given sample, appears independent of $T$. The present measurements are insufficiently detailed to permit the separation of the possible temperature dependence of $t_{ono}$, $t_o$ and $V_c$, but it seems likely that decreasing $T$ results in an increase in $V_c$, with $t_{ono}$ being relatively unaffected. The parameters $V_c$, $t_o$ and $t_{ono}$ are found to lie in the range 10-15V, 10-50$\mu$s and 0.1 to 0.3$\mu$s respectively, at 295K.

The detailed behaviour of $t_{on}$ with $V$ at the extremes of the voltage range is difficult to establish. As $V \sim V_c$ there is a
Figure 7.18 The dependence of the onset time $t_{on}$ with pulse height $V$ and temperatures for a-Si:H p$^+$-n-i structure (ASi99).
tendency for \( t_{on} \) to become erratic, but no current instabilities have yet been recorded with \( t_{on} > 100\mu s \). Thus it is concluded that either \( t_{on} \) increases almost discontinuously at \( V \sim V_c \), or the effect simply does not occur under such conditions. As \( V \) is increased several volts above \( V_c \), the curve flattens, i.e. \( t_{on} \sim t_{ono} \). It is worth pointing out that this behaviour is similar to that illustrated in the delay time versus applied voltage curve in figure 7.12 where \( V > V_{CR} \). It should be noted that the total sample thicknesses are substantially different in figures 7.12 and 7.18 (cf. xSi262 and ASi99 in Table 7.1). For devices with thin i-layers (e.g. ASi99), further increasing \( V \) ultimately causes an irreversible change in the device characteristics. There is an abrupt increase in current, and the device remains in a permanent low resistance state \( (10^2 - 10^4 \Omega) \) state when the voltage pulse is removed.

The rise and fall times of the current instability as a function of \( V \) for a typical sample (ASi99) are shown in figure 7.19. The current decay is essentially exponential, as illustrated in figure 7.20, and \( \tau_i \) is the time constant of this decay. The form of the current rise is less clear, and in this case \( \tau_i \) denotes the time taken for the current to increase from 10\% to 90\% of \( I_{\text{max}} \).

The variation of \( I_{\text{max}} \) with \( V \) for three identically prepared samples with differing areas is shown in figure 7.21. It can be seen that in each case \( I_{\text{max}} \) scales linearly with \( V \) \( (V > V_c) \), but is not correlated with sample area. Measurements on a large number of
Figure 7.19 The rise ($\tau_r$) and fall ($\tau_f$) times of the current instability as a function of $V$ for a-Si:H $p^+\text{-}n\text{-}i$ structure (ASi99).
Figure 7.20 The current decay of the instability of a-Si:H p-n-i structure (ASI99), note that $\tau_f$ is the time constant of this decay.
Figure 7.21 The variation of $I_{\text{max}}$ with $V$ for three identically prepared samples (ASi99) with differing contact areas as shown.
samples with areas varying by three orders of magnitude failed to reveal a scaling of $I_{\text{max}}$ (measured at a constant $t_{\text{on}}$) with contact area, as shown in figure 7.22. It should also be mentioned that the critical voltage $V_c$ shows a tendency to decrease with increasing area.

Initial observations indicated that at voltages slightly above $V_c$ only a single current instability would propagate through the sample, even if the voltage pulse was maintained for orders of magnitude longer than the onset time $t_{\text{on}}$. However, during the course of these measurements, a sustained voltage was often found to cause an abrupt change to a permanent low resistance state. In order to minimise the risk of this occurring during a series of measurements, two voltage pulses of equal height and width were used to determine the time which must elapse for the second pulse to give rise to a current instability with similar values of $t_{\text{on}}$ and $I_{\text{max}}$ to the first (the recovery time $t_r$). The variation of $t_r$ with pulse height $V$ is shown in figure 7.23.

At voltages substantially above $V_c$, i.e. where $t_{\text{on}}$ approaches $t_{\text{ono}}$, the current decay associated with the first voltage pulse was frequently observed to behave erratically, contrary to the trend shown in figure 7.19. Under these conditions $t_r$ was found to be commensurate with $t_{\text{on}}$, and local maxima could occasionally be seen shortly after the initial current rise.

In addition to the abrupt changes in the electrical properties of samples which have been mentioned above, less obvious
Figure 7.22 The variation of $I_{\text{max}}$ with differing contact areas of identical a-Si:H p'-n-i samples (ASi99).
Figure 7.23 The variation of the recovery time ($t_r$) with pulse height $V$ for a-Si:H $p^−$-ni structures.
irreversible changes were also found to occur. These effects are manifested particularly in the period prior to the onset of the current instability, taking the form of a progressive increase in the current with successive constant amplitude voltage pulses. This increase is more pronounced when voltage pulses substantially above $V_c$ are applied. Prior to the point at which this becomes noticeable, the pre-instability current, $I_s$, is approximately exponentially dependent on the applied voltage and scales linearly with sample area. Typical I-V characteristics of a sample which has undergone progressive changes is shown in figure 7.24. It can be seen that the forward biased ($p^+$ positive) characteristic is substantially modified but the reverse biased ($p^+$ negative) characteristic is essentially unaltered.

§7.3 ON- and OFF-states

§7.3.1 Comparison of virgin, ON- and OFF-states

It was shown in §7.1.4 and 7.2.5 that the J-V characteristics of devices with Cr W$_1$-i contacts exhibit certain properties that are significantly different from devices with Al contacts. Although they form at similar voltages, devices with Al W$_1$-i contacts (type A) usually form directly to a low resistance state while devices with Cr contacts (type B) sometimes need several pulses to reach a low resistance.
Figure 7.24 Typical static I-V characteristics of a-Si:H p⁺-n-i structure (ASi99) which has undergone progressive changes. Note that the forward biased characteristic has increased while reverse biased characteristic is essentially unaltered.
The ON-state I-V characteristic of a type A device is linear and symmetric, as shown in figure 7.25, unless it happens to be in one of the limited number of intermediate states (e.g. states such as e or f in figure 7.1). It appears that the I-V characteristics of type B devices, in any resistance state after forming, are approximately symmetric but the degree of non-linearity is a function of the sample resistance (see figure 7.15).

The virgin and OFF-state I-V characteristics of a typical type A device (ASi131) are shown in figure 7.26. Although they resemble one another fairly closely, it is worth noting that deviations from ohmic behaviour occur at lower voltage in the formed OFF-state. For type B devices it appears that there is no well defined OFF-state (see §7.2.5) and there is no similarity between the post-forming I-V characteristic of a high resistance state and the virgin I-V characteristic.

§7.3.2 Temperature sensitivity of resistance states

The temperature dependence of the ON-state resistance of type A devices was measured for a number of specimens over the range 200K to 400K. In all cases the resistance changed very little with temperature, generally decreasing by less than 10% on going from 200K to 400K. If the ON-state resistance were supposed to be thermally activated, i.e.

$$ R = \exp \left( \frac{E}{kT} \right) $$

(7.2)
Figure 7.25 I-V characteristics of a type A devices (xSi268) in the ON-state, at different temperatures, in the forward and reverse directions.
Figure 7.26 A comparison of the I-V characteristics of type A (ASi131) (a) virgin and (b) formed OFF-state devices.
then $\epsilon$ would be much less than $kT$. The temperature dependence of the OFF-state resistance was generally found to be of the form:

$$ R = R_0 \exp\left[\frac{\epsilon}{kT}\right] $$  \hspace{1cm} (7.3)

where $\epsilon$ was a few tenths of an eV but varied from sample to sample.

A limited number of resistance($R$) versus temperature($T$) measurements were made on type B devices(7). It seems that type B devices in an ON-state are more sensitive to temperature than type A. Further experiments are needed to extend the measurements for $R > 50k\Omega$, and to determine whether the temperature sensitivity is a systematic function of $R$. As far as can be ascertained, there is little evidence for thermal activated processes in the ON-state conduction of type B devices.

§7.3.3 ON- and OFF-state resistances - area dependence

Figure 7.27 shows the area dependence of the formed OFF-state resistance, $R_{OFF}$, for type A devices of different areas, fabricated from a single $p^+-n-i$ deposition. These results were obtained on specimens that had previously been switched many times. Within the experimental scatter, $R_{OFF}$ clearly scales with the reciprocal of the area demonstrating that in the OFF-state, the current flows uniformly across the whole area of the specimen (as in the virgin state - see §7.1.5).

In complete contrast, the ON-state resistances, $R_{ON}$, for the
Figure 7.27 Area dependence of a type A device (ASi82) OFF-state resistance. Note that $R_{\text{OFF}}$ has the same values as in the virgin states shown in figure 7.8.
same specimens show no area dependence at all as can be seen from figure 7.28. This result can be understood only if the ON-state has its origin in a conducting filament, less than a few μm in diameter, that extends at least part of the way through the specimen thickness. This result, although not entirely unexpected, will obviously be of central importance in developing a model for the switching process. A direct proof of the existence of a filamentary ON-state is provided by the results in §7.3.4.

§7.3.4 Observation of ON-state filament

In order to learn more about the ON-state a series of experiments were carried out in which the surface of the device was covered with a thin layer of a thermochromic liquid crystal(7). By passing current through the device in the ON-state it is possible to observe the current path from the changes produced by Joule heating in the reflected colour of the liquid crystal(7). The results obtained by the Dundee group for two 20μm diameter surfaces, viewed through a high power optical microscope are shown in figure 7.29. Figure 7.29(a) shows the liquid crystal surface in the absence of any current flow through the specimen and figure 7.29(b) shows a sample with current flowing in the ON-state. The change in the liquid crystal appearance produced by Joule heating within the filament can be clearly seen. Figure 7.29(c) represents another device through which a larger current has been passed. From a number of measurements it was estimated visually that the ON-state is
Figure 7.28 Area dependence of the ON-state resistance $R_{ON}$ of $p^+\text{-}n\text{-}i$ type A devices (ASi82).
Figure 7.29 (a) Photograph of a 20μm diameter a-Si:H memory structure covered with a liquid crystal layer. The arrow indicates the position of the ON-state filament.
(b) Photograph of a similar structure to that shown in (a). The ON-state filament, indicated by the arrow, has been made more visible by passing a larger current through it.
(c) A even more clearer (i.e. more current than (b)) picture of the filament.
associated with a filament of maximum diameter 0.5µm. This result has interesting implications for the understanding of the switching process. Visual observation of the current filament has also established that switching a device OFF and ON again produces the current filament in the same place and this implies that the switching process is not destructive.

In another series of experiments at Edinburgh University† the specimens were covered by a thin layer of liquid crystal, 4-cyano-4alkylbiphenyl, which undergoes a nematic-liquid phase transition at 35.3°C. The phase boundary may be observed easily in cross-polarised light and the transition was found to be fast and without hysteresis. If the sample temperature is fixed using a thermostatically controlled stage, the difference in temperature between a region of local heating and the surrounding film may be determined. The results indicated that no observable temperature rise occurred as a result of applying electrical power to the pore in either the virgin state just prior to forming, or in the formed OFF-state just prior to switching. However, as described above, in the ON-state local heating, which results on applying continuous electrical power, could be clearly seen. The effect of changing the RMS power applied to a 50µm diameter pore was studied using a continuous train of 300ns pulses. The stage was maintained at 21°C, thus the phase transition represents the locus of point (35.3-21)=14.3°C above the film temperature. The isotherms were circular

† Carried out by Drs J. Hajto and S. Reynolds of the Electrical Engineering Department, University of Edinburgh.
and in the particular case studied were symmetric about the centre of the pore.

A plot of the phase boundary diameter $d_1$ versus RMS power $P$ is shown in figure 7.30. Although there is considerable scatter it can be seen that the relationship between $d_1$ and $P$ is substantially linear for $d_1 > 2 \mu m$. Below this the accuracy of the measurements is limited by the resolution of the microscope. A linear dependence of $d_1$ on $P$ is obtained as a solution of the heat conductivity equation for an idealised system of this kind, in which the source of local heating is assumed to be much smaller than $d_1$. Thus, these data indicate that the diameter of the ON-state filament must be less than $2 \mu m$, in agreement with the above experiments.

Experiments have also been carried out to locate the conducting filament using SEM and X-ray microprobe techniques. The SEM photographs of formed pores reveal changes in the surface morphology. These areas are craterous and variable in size and it is usual to observe changes in the surface morphology immediately after forming. Furthermore the centre of the "hot spot", as verified by the liquid crystal technique, usually corresponds to the area of the surface changes indicating the presence of the localised electrical conduction (filament) at these sites.

The SEM and X-ray microprobe analysis were carried out on a number of $p^+\cdot n\cdot i$ pore structures by the Dundee group. They were formed and switched ON and OFF several times and then the Cr $p^+\cdot i$ (top) electrode was removed. From the X-ray microprobe analysis on
Figure 7.30 Plot of the diameter $d_1$ of the ON-state as a function of the RMS power $P_{RMS}$, measured at constant pulse height and variable mark-space ratio (sample AS193).
the exposed pore area, there is no Cr signal as the top Cr contact had been removed. However, in the area where surface changes were exhibited (indicated by SEM pictures) a Cr signal was observed. This device was in the OFF-state immediately prior to the removal of the Cr electrode but similar results were obtained for devices in the ON-state.

These results indicate that the ON-state of the a-Si:H structures might be associated with a conducting filament containing Cr or Cr-silicide tracks or islands shorting out the intrinsic i-layer. It is worth pointing out that the temperature dependence of the ON-state resistance (see §7.3.2) rules out simple metallic conduction but tunnelling between metallic Cr or Cr-silicide islands for ON-state conduction is at least a possibility.

§7.3.5 Magnetoresistance

Transverse magnetoresistance measurements of the ON-state have been carried out by the Dundee group, at room temperature and fields (B) of 0.5T. Within experimental error, the magnetoresistance ratio \( \Delta \rho/\rho \) is proportional to \( B^2 \) and is positive. The quotient \( \Delta \rho/(\rho B^2) \) ranged from \( (0.5 \text{ to } 2) \times 10^{-4} \ T^{-2} \). Experiments on phosphorus doped a-Si:H after thermal crystallisation also gave a positive magnetoresistance with the same \( \Delta \rho/(\rho B^2) \) dependence. Unfortunately, no results on homogeneous undoped glow

\[ \Delta \rho = \text{positive} \]

\[ \rho = \text{resistance} \]

\[ B = \text{magnetic field} \]

\[ \text{dependence} \]

\[ \text{results} \]

\[ \text{available} \]

† The author is grateful to Prof. W.E. Spear of Dundee University for making these results available.
discharge a-Si:H films have been reported. It is therefore difficult to draw any definite conclusions about the amorphous or crystalline nature of the ON-state filament from the present results.
References


(6) To be published.

§8.1 The virgin state

The static I-V characteristics of virgin a-Si:H $p^+\text{-}n\text{-}i$ memory devices show marked polarity and temperature dependence and they depend upon several device parameters, such as the thickness ($d_n$), the doping level of the n-layer and the metal($M_1$)-i contact. It was shown in §7.1.2 that there seems to be a critical n-layer thickness ($d_{n\text{CR}}$) below which the I-V characteristics of a sample with $d_n < d_{n\text{CR}}$ are essentially the same as for a $p^+\text{-}i$ structure (i.e. n-layer thickness is zero). For particular $p^+\text{-}n\text{-}i$ devices with doping levels of $10^4$ vppm for the $p^+$-layer and 30 vppm for the n-layer, $d_{n\text{CR}}$ is estimated to be ~300nm. The existence of $d_{n\text{CR}}$ is also supported by the capacitance-voltage (C-V) measurements at 1 MHz (see §7.1.6) on $p^+\text{-}i$ and $p^+\text{-}n\text{-}i$ structures. The C-V characteristics of samples with $d_n < d_{n\text{CR}}$ are similar to those of $p^+\text{-}i$ structures while structures with $d_n > d_{n\text{CR}}$ have similar characteristics to crystalline silicon MIS devices. It should be noted that all of these experiments (i.e. the I-V in §7.1.2 and C-V in §7.1.6) were carried out with aluminium ($M_1$) top contacts because the $M_1$-i contact ($\S$7.1.4) also affects the I-V measurements substantially, especially in forward bias.

From figure 7.4, it can be seen that for $d_n > d_{n\text{CR}}$, the I-V
characteristics can be divided into three regions, i.e. the ohmic region at low applied voltages, an \( I \propto V^2 \) region at moderate bias and \( I \propto V^m \), where \( m > 2 \), at high applied bias.

In §3.3.1, a brief discussion of one carrier space-charge-limited current (SCLC) was presented. It was shown that for one carrier SCLC to prevail, a region of \( J \propto V^2 \) should be evident in the J-V dependence. If the current is bulk limited, a plot of \((V/d^2)\) versus \((J/d)\) (where \( d \) is the sample thickness) should be the same for different sample thicknesses. Mackenzie et al(1) have presented an SCLC analysis of data obtained from a-Si:H \( n^+-i-n^+ \), or \( n^+-n-n^+ \) structures, and show that the dominant level controlling the SCLC is always situated close to the quasi-Fermi level. The density-of-states obtained from such a model also proved satisfactory.

In this work, it was found that at low bias, the I-V dependence was ohmic and at moderately high forward bias, the \( p^+-n \) junction is fully on and the \( M_i \) Schottky junction is reverse biased; the holes from the \( p^+-n \) junction are injected into the \( n^- \) and \( i \)-layers and constitute the current flowing through the structure. Although multi-layer structures are considered here, the thickness scaling rule is satisfied in the \( p^+-n-i \) structures (see below), and as a consequence the one carrier SCLC model is valid.

The J-V characteristics of ASi33, xSi543 and xSi316 are plotted on a log J versus log V scale in figure 8.1. It can be seen from figure 8.1 that region A shows a \( J \propto V^2 \) relationship for the samples with thicker \( n \)-layers. The \((V/d_n^2)\) versus \((J/d_n)\) plot for these
Figure 8.1 Log J versus log V plots for a-Si:H p⁺-n-i devices with different n-layer thicknesses. Some of the data are quoted from figure 7.4.
samples is shown in figure 8.2. It should be noted that only the n-layer thickness is being varied here and it follows from figure 8.2 that the scaling law of the one carrier SCLC model is satisfied for samples with \( d_n > d_{nCR} \) but not when \( d_n < d_{nCR} \).

Having satisfied the conditions for one carrier SCLC conduction, the trap density \( (N_t) \) can be calculated from the following equation (2):

\[
N_t = \frac{\epsilon_x \epsilon_o V_x}{e d_n^2} \quad (8.1)
\]

where \( V_x \) is the voltage at which the J-V characteristic changes from ohmic to SCLC flow (marked C in figure 8.1), \( e \) is the electronic charge, \( \epsilon_o \) is the free space dielectric constant and \( \epsilon_x \) is the relative dielectric constant. The trap densities of xSi316, xSi543 and ASi9 are obtained by adopting \( \epsilon_x = 12 \) for n-type a-Si:H and are tabulated in Table 8.1.

As shown in Chapter 2 (§2.1) the density of gap states for GD deposited n-type a-Si:H of 30 vppm PH\(_3\) is approximately \( 6 \times 10^{17} \) cm\(^{-3}\) ev\(^{-1}\), deduced from the field effect measurements. However, Mackenzie et al (1) have obtained a density of states using the one carrier SCLC model in the range \( 1.2 \times 2 \times 10^{17} \) cm\(^{-3}\) ev\(^{-1}\) which is 3 - 5 times lower. This discrepancy was explained by the fact that the density-of-states in the surface region probed by the field effect is higher than the average density-of-states obtained by a volumetric (i.e. SCLC) method. It can be seen from Table 8.1 that,
Figure 8.2 A $J/d_n$ versus $V/d_n^2$ plot for samples AS19($\square$), xSi543(○) and xSi316(○). Note $d_n$ is the effective n-layer thickness.
Table 8.1 The calculated trap density \( N_t \) for three a-Si:H p'-n-i samples using one carrier SCLC analysis.

<table>
<thead>
<tr>
<th>sample</th>
<th>( N_t (\text{eV}^{-1} \text{cm}^3) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>xSi316</td>
<td>( 1.06 \times 10^{16} )</td>
</tr>
<tr>
<td>xSi543</td>
<td>( 4.61 \times 10^{16} )</td>
</tr>
<tr>
<td>ASi9</td>
<td>( 4.59 \times 10^{16} )</td>
</tr>
</tbody>
</table>
within an order of magnitude the estimated trap density by the one
carrier SCLC model for the p⁺-n-i structures where \( d_n > d_{nCR} \) is
close to that reported in the literature.

In a p⁺-n-i structure where the p⁺-layer is heavily doped (10⁴ vppm) and
the n-layer is lightly doped (30 vppm), the depletion layer of the p⁺-n
junction will extend predominantly into the n-
region. From §2.3.1, \( (\varepsilon_c - \varepsilon_f)^p \approx 1.2\text{eV} \) for the p⁺-layer and
\( (\varepsilon_c - \varepsilon_f)^n \approx 0.3\text{eV} \) for the n-layer. An example, in §2.4.2, for an a-
Si:H p-n junction with \( (\varepsilon_c - \varepsilon_f)^p = 0.35\text{eV} \) and \( (\varepsilon_c - \varepsilon_f)^n = 1.25\text{eV} \) gave
a depletion layer of approximately 100nm. It was shown in §2.4.1
that the space charge depletion layer of a metal-intrinsic a-Si:H
Schottky barrier (i.e. Mᵢ-i junction), with \( (\varepsilon_c - \varepsilon_f)_n = 0.8\text{eV} \) for the
undoped i-layer, can be of the order of 200nm. These figures agree
well with the observation that for these particular doping levels
for the p⁺-n-i structure (i.e. 10⁴-30-0 vppm) there is a critical
n-layer thickness \( (d_{nCR}) \) which is about 300nm. For a given p-layer
doping (10⁴ vppm in all of the present samples) therefore, \( d_n \) must
be > 300nm before any influence of the n-layer thickness would be
expected (e.g. on SCLC).

The doping level of the n-layer is very important. Figure 8.3
shows a log \( J - \log V \) plot for three samples with two different n-
layer doping levels (cf. §7.1.3). For samples ASi94 and ASi93 there
is no \( J \propto V^2 \) dependence and since the n-layer is more heavily doped
in these two samples, the depletion layer in the n-side of the p⁺-n
junction should decrease, and provided the Mᵢ-i contact is the same
Figure 8.3 Log J versus log V plots for a-Si:H p⁺-n-i devices with different n-layer doping levels. Note data are quoted from figure 7.6.
then $d_{nCR}$ should reduce rather than increase as observed experimentally. However, the effective n-layer (i.e. the n-layer between the $p^+-n$ and the $n^{-}-i$ junctions), which is heavily doped (202 vppm), has a conductivity of $10^{-5} \ \Omega^{-1} cm^{-1}$. Thus it is perhaps not surprising that $d_{nCR}$ is increased as the n-layer with 30 vppm has a conductivity of $10^{-3} \ \Omega^{-1} cm^{-1}$. Also the absence of $J \propto V^2$ in figure 8.3 suggests that SCLC does not occur in samples with heavily doped n-layers. Note that the $n^+-n-n^+$ structures used by Mackenzie(3) for the SCLC measurements had n-layers with at the most 15 vppm dopant.

The log $J$- log $V$ characteristics of region B in figure 8.1 are replotted in figure 8.4 as log conductivity ($\sigma$) versus square root of field ($E^{1/2}$). It can be seen that the conductivity prior to forming is proportional to the square root of the applied field. There are at least two conduction mechanisms (i.e. the Schottky and the Poole-Frenkel effects, see §3.3.2) which can give rise to nonohmic behaviour of this form.

Simmons(4) pointed out that although the functional dependence of the conductivity upon field strength is the same for the Schottky and the Poole-Frenkel effects, it is possible to differentiate these two effects from the derived value of the relative dielectric constant ($\varepsilon_r$). The relative dielectric constant can be deduced from the slope ($\beta_s/kT$ or $\beta_{pf}/kT$) of the log $\sigma$ versus $E^{1/2}$ plot:

$$\beta_s = \left[ \frac{e^3}{\pi \varepsilon_0 \varepsilon_r} \right]^{1/2} \quad (8.2)$$
Figure 8.4 The log $\sigma$ versus $E^{1/2}$ plots for a-Si:H $p^+-n-i$ devices with different n-layer thicknesses. Some of the data are obtained from figure 7.4.
The slope of figure 8.4 is $0.42 \times 10^{-3}$ V cm$^{-1}$ and hence $\varepsilon_\infty$ obtained for the Poole-Frenkel effect is 48.7 and for the Schottky effect is $\sim$12.2. The relative dielectric constant for crystalline silicon is about 12 and this value does not change very much with frequency(5). Assuming that the relative dielectric constant for amorphous silicon is similar to that of crystalline silicon, it seems that the current flow in region B of figure 8.1 (just prior to switching to the first ON-state) is determined by the Schottky effect at the $\text{M}_1$-$i$ contact. This is consistent with the experimental observation that the $\text{M}_1$-$i$ contact substantially affects the forward biased I-V characteristics of a-Si:H $p^+$-$n$-$i$ structures (see §7.1.4).

The capacitance-voltage (C-V) measurements on a-Si:H virgin devices also exhibit a similar dependence on the n-layer thickness as described §7.1.6. The C-V plots of the $p^+$-$i$ structures resemble the C-V characteristics of an MOS capacitor, which is not surprising as the structures are essentially quite similar. This also implies that $p^+$-$n$-$i$ structures with very thin n-layers should give similar C-V characteristics to those of $p^+$-$i$ structures because in thin n-layer devices, the n-layer is almost "non-existent", as suggested in the previous paragraph.

To describe the C-V characteristics of $p^+$-$n$-$i$ structures with $d_n > d_{\text{nCR}}$, it is instructive to examine the C-V plots of c-Si MISS devices presented in §5.2.3. The capacitance of the c-Si MISS device

$$B_{\text{pf}} = \left[ \frac{\varepsilon}{4 \pi \varepsilon_0 \varepsilon_\infty} \right]^{1/2}$$

(8.3)
in the OFF-state is considered to be the sum of three capacitances in series, i.e. the capacitance of the insulator $C_1$, of the surface depletion layer $C_s$, and of the p-n junction $C_j$. With negative polarity, the p-n junction is reverse biased and the M-i-n part of the device is in a state of accumulation. In this condition a considerable part of the bias voltage is dropped across the reverse biased p-n junction, $C_j$ is dominant, and the C-V characteristics are similar to those of a reverse biased p-n junction. The capacitance $C_j$ increases when the p-n junction is forward biased and simultaneously $C_s$ gradually increases as the M-i-n portion goes into depletion. The characteristics show the depletion layer capacitance similar to MIS diodes. Bearing in mind that the a-Si:H p+ \text{-} n-i structure is an analogue of its crystalline counterpart, it is possible that similar mechanisms to those operating in c-Si MISS structures can be applied to a-Si:H MISS structures. However, it should be borne in mind that the derivation of the depletion widths of both the p-n junction and the Schottky barrier is different in the amorphous case as outlined in §2.4.1 and 2.4.2.

The above argument is consistent with the description presented in the discussion of $d_{\text{nCR}}$ where the p-n and M-i-junctions are considered. Finally, it should be mentioned that only devices with aluminium (Al) contacts were used in the C-V measurements and it would be interesting to try other M-i contacts.
§8.2 The forming process

It was shown in §7.2.2 that the forming delay time ($t_D$) is an extremely sensitive function of the applied voltage and it varies over nearly ten orders of magnitude from a few hundred seconds at low forming voltages to about 10 ns at high voltages. When a sufficiently high forward bias voltage pulse is applied across the a-Si:H $p^+-n-i$ structure, the $p^+-n$ junction should almost instantaneously turn "ON", thus supplying ample holes to the $n$-layer. Under these conditions the $n_i$ contact is reverse biased which implies that the $n_i-i$ junction is near breakdown and most of the applied voltage should drop across this junction. The transit time ($t$) for a hole to pass through the $n$-layer can be estimated as follows:

$$t = \frac{d_n}{\mu E}$$

(8.4)

where $d_n$ is the $n$-layer thickness, $\mu$ is the mobility of holes and $E$ is the electric field across the $n$-layer. Under forward bias there will be a depletion layer at the $n_i-i$ contact which will extend into the $n$-layer as estimated earlier. By assuming that this depletion layer which extends into the $n$-layer is small compared with $d_n$, and also that most of the voltage is dropped across the $n_i-i$ junction, an estimation of the transit time of holes can be performed using equation (8.4). Taking $d_n = 500$nm, $\mu = 0.001$ cm$^{-2}$V$^{-1}$s$^{-1}$ (6) and $E \sim 10^5$ V cm$^{-1}$, the transit time $t = 500$ns which is consistent with the experimental observation that $t_D$ tends to a value of
In §7.2.3 it was found that $V_F$ does not extrapolate to zero voltage as $d_n \to 0$ and the intercept of figure 7.13 (i.e. a $V_F$ versus $d_n$ plot) is approximately 15V. It is reasonable to assume that this voltage drop can be attributed to the breakdown voltage of the $M_1$-$i$ junction. If the doping level of 30 vppm is considered lightly doped, it is reasonable to compare the "punch-through" model developed for c-Si MISS devices with the results obtained from the a-Si:H devices. From §5.3.1 the switching voltage ($V_S$) can be written as:

$$V_S = q \frac{(d_n - d_j)^2}{N_D \frac{2 \varepsilon_x}{\varepsilon_o}}$$

(8.5)

where $d_n$ is the thickness of the n-layer and $d_j$ is the distance which the depletion region of the $p^+$.n junction extends into the epitaxial layer. As discussed earlier for a-Si:H $p^+$.n-$i$ structures with $10^4$-30-0 vppm doping levels, there seems to be an effective depletion layer of 300nm, so $d_j$ should be around 300nm. Taking $\varepsilon_x=12$ and $N_D = 10^{17} \text{cm}^{-3}$, $V_S$ values for $p^+$.n-$i$ structures with different n-layer thickness are tabulated in Table 8.2. Note that the total voltage ($V_T$) across the device should be the sum of $V_S$ plus the voltage across the $M_1$-$i$ junction ($V_{mi}$). If $V_{mi} = 15V$, a tentative forming voltage ($V_F$) versus $d_n$ relationship for a-Si:H $p^+$.n-$i$ structures can be calculated. A range of values are shown in Table 8.2.
Table 8.2 The calculated forming voltage ($V_F$) for different effective n-layer thicknesses derived from the "punch-through" model (detail see §8.2).

<table>
<thead>
<tr>
<th>effective n-layer (nm)</th>
<th>$V_s$ (v)</th>
<th>$V_F$ (v)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>0.75</td>
<td>15.75</td>
</tr>
<tr>
<td>500</td>
<td>3</td>
<td>18</td>
</tr>
<tr>
<td>600</td>
<td>6.75</td>
<td>21.75</td>
</tr>
<tr>
<td>700</td>
<td>12</td>
<td>27</td>
</tr>
<tr>
<td>800</td>
<td>15.75</td>
<td>30.75</td>
</tr>
<tr>
<td>900</td>
<td>27</td>
<td>42</td>
</tr>
</tbody>
</table>
The "forming" voltages tabulated in Table 8.2 are plotted together with the experimental data from figure 7.13 in figure 8.5. It can be seen that the predicted "forming" voltages do not agree with the experimental results. However it should be noted that equation (8.5) is developed for crystalline devices and it is unlikely that the same calculations are directly applicable to amorphous MISS devices. As was discussed in §2.4, for example, there are significant differences in the depletion profiles of c-Si and a-Si:H p-n junctions. A more rigorous derivation of equation (8.5) for the amorphous case would be helpful.

The measured forming voltages, $V_F$ also do not scale linearly with the i-layer thickness ($d_i$) as might be expected from a simple field dependent mechanism (see §7.2.4). If the estimation of the depletion layer of the $M_i$-i contact in §8.1 is valid, then it is certain that in all the samples used in this project (see Table 7.1 for i-layer thicknesses) the i-layer is completely depleted, even at zero bias. The forming process is so complicated however (see later for a more comprehensive discussion) that it would be surprising if a linear relationship were found between $V_F$ and $d_i$.

The area dependence experiments in §7.1.5 show that in the virgin state the current flows uniformly throughout the entire area of the specimen but as reported in §7.2.4, the forming voltage is insensitive to contact area suggesting that at high applied bias, current is flowing in a predetermined path.

The current instabilities phenomena reported in §7.2.6 in
Figure 8.5 A comparison of the forming voltages deduced from the "punch-through" model (o) and the experimental data for the a-Si:H p'-n-i devices.
virgin \( \text{p}^+\text{-n-i} \) structures with thin i-layers (<10nm) also exhibit similar behaviour. The absence of a pronounced dependence of \( I_{\text{max}} \) upon contact area (e.g. figure 7.22) suggests that the current instabilities occur in a localised region and, as the smallest device used in this project is of the order of 10\( \mu \text{m} \) in diameter, the majority of the current during the instability must be transported through a region of these dimensions or less. It is interesting to note that the shape of the onset time \( t_{\text{on}} \) versus voltage curve (figure 7.18) at high applied bias is similar to the delay time \( t_D \) versus applied voltage results (figure 7.12) discussed earlier. On this basis it seems reasonable to suppose that the current instability is a precursor to forming, although there is no direct evidence to support this. Indeed there are certain indications that these events may be only indirectly related, as a current instability is not always observed prior to forming in the samples described in §7.2.2, and very seldom in samples with thicker i-layers.

It is interesting to note that current controlled negative resistance (CCNR) was rarely observed under static conditions prior to forming, as discussed in Chapter 4. It appears that a-Si:H structures cannot support high local current densities (and consequent Joule heating) for more than a short time before a permanent change in the material occurs. The progressive changes in the static I-V characteristics (§7.2.6) tend to substantiate this view.
There is no acceptable model for these phenomena at present but the following discussion outlines possible approaches to an explanation. The $t_D$ and $t_{on}$ versus voltage data at room temperature for a-Si:H (figures 7.12 and 7.18) and c-Si (figure 5.4) MISS devices (data taken when $I_B = 0$) are plotted in figure 8.6. These data follow a similar pattern which indicates that the principles on which c-Si MISS devices are based may be applicable to the a-Si:H structures, although some modifications must be anticipated.

Tentative band diagrams for the a-Si:H $p^+\text{-n}\text{-i}$ structure at zero, moderate and high applied bias are shown in figure 8.7. Under zero bias (figure 8.7(a)) the $N_1\text{-i}$ interface represents a Schottky barrier in which the i-layer and part of the n-layer is depleted. The equilibrium currents $i_e$ and $i_h$ originate from thermionic emission over the Schottky barrier and hole diffusion from the $p^+$-layer respectively. If a moderate bias is applied (figure 8.7(b)), the electrons from $N_1$ can tunnel into the conduction band, adding to the thermionic current. However, the $p^+\text{-n}$ junction is not substantially forward biased and the hole current will be comparable to the electron tunnel current. As the field in the n-region is small the holes will gradually diffuse towards $N_1$.

Under high bias conditions (figure 8.7(c)) the electron tunnel current will be substantial, as the effective barrier width is further reduced. In addition, hole injection will increase as a result of a larger forward bias on the $p^+\text{-n}$ junction. It is possible that the increased hole injection gives rise to a positive space charge in the vicinity of the $N_1\text{-i}$ interface which will further
Figure 8.6 A comparison of $t_D(x)$ and $t_{on}(o)$ of a-Si:H devices and the $t_D(o)$ of c-Si HISS devices versus applied voltage.
Figure 8.7 Tentative band diagrams for the a-Si:H p⁺-n-i structures at (a) zero bias, (b) moderate bias, (c) high bias.
reduce the effective tunnelling barrier by its electrostatic effect. This would account for an abrupt increase in the measured current after a delay time if it is considered that the positive space charge takes approximately \( t_D \) or \( t_{on} \) to build to some critical level.

This rapid rise in current may be a consequence of the high energy tunnelling electrons causing impact ionisation, and leading to an avalanche breakdown. Such effects are known to occur widely in dielectric films and reverse biased p-n junctions(7). Furthermore, avalanche breakdown in p-n junctions occurs in local high field regions which is in accord with our observations of a weak dependence of \( I_{max} \) on sample area. However, avalanche breakdown is a statistical process(7), and thus if this were to be the primary origin of the observed \( t_{on} \) or \( t_D \) one would expect little correlation between this parameter and the applied voltage. This does not appear to be the case and therefore it is suggested that \( t_{on} \) or \( t_D \) is governed by the more predictable mechanism of hole accumulation.

The observed relationships between \( t_D \) and \( V \) or \( t_{on} \) and \( V \) and temperature can be explained qualitatively by assuming that just prior to a rapid rise in current (i.e. forming, or a current instability is observed) a critical charge \( Q_C \) must be obtained. Below \( V_{CR} \) or \( V_C \), the \( p^+\)-n junction cannot supply sufficient holes to offset conduction and recombination, and \( Q_C \) is never reached. Above \( V_C \), the supply of holes is increased by virtue of a larger forward bias appearing across the \( p^+\)-n junction and after a certain time...
(i.e. \( t_{on} \) or \( t_D \)) \( Q_C \) is reached and a large electron current occurs. As the hole injection current is exponentially dependent on the \( p^+\)-\( n \) junction bias it is reasonable that the time taken for \( Q_C \) to develop should behave as depicted in figure 8.6, i.e. following the empirical relationship (see §7.2.6):

\[
t_{on} = t_{ono} + t_o \exp \left[ \frac{-(V-V_C)}{V_o} \right]
\]  

(8.6)

assuming a fixed proportion of the total applied bias with \( V > V_C \) (or \( V > V_{CR} \)) appears across the \( p^+\)-\( n \) junction. The existence of a minimum value of \( t_{on} \) (or \( t_D \)) can be explained by considering the time taken for a large hole current, sufficient to result in \( Q_C \), to diffuse through the \( n \)-layer. Note that this postulation is in complete agreement with the earlier SCLC analysis. Increasing the temperature will increase the hole saturation current, and consequently a smaller forward bias will provide sufficient hole injection for \( Q_C \) to be reached at a lower \( V_C \) provided recombination in the \( n \) and \( i \) regions is not substantially altered. It should be noted that only a transient high conducting state is usually observed in the thin \( n \)-layer \( a\)-\( Si:H \) \( p^+\)-\( n \)-\( i \) structures and a permanent ON-state (first ON-state) is obtained from samples with thick \( n \)-layers, after \( t_D \) (i.e. after forming).

As the current increases abruptly (figure 8.7(c)) a large density of electrons is injected into the \( n \) region, and consequently the possibility exists that the holes constituting the positive space charge will recombine with these injected electrons. If this
were to occur then it is to be expected that the measured current will decrease as the barrier will then become less transparent to electrons.

As mentioned in §5.2.7, Adan and Zolomy report that the threshold voltage for c-Si MISS samples decreases as the frequency of the applied voltage pulses is increased. They attribute this effect to a residual charge being stored at the n-i interface and a diffusion charge extending through the n-layer from the p^+\text{-}n junction to the interface. This stored charge is released on a time scale of microseconds, and thus if the period of the applied pulse train is of this order the effective threshold voltage will be reduced. Unfortunately the same experiment cannot be carried out on the a-Si:H devices as they undergo rapid changes in the low bias I-V characteristic and will very often form when a continuous train of pulses is applied. However, the 'two pulse' technique that was described §7.2.6, is essentially identical inasmuch as any charge storage effect of this kind should be apparent from the current response of the second pulse. One would expect \( t_{on} \) to decrease as a result. From the present data it would appear that \( t_{on} \) is actually increased after the first current instability, and it follows that an equivalent charge storage model is inappropriate. However, as there will be substantial electron injection from the metal at the onset of conduction, it is possible that a residual electron charge will remain trapped close to the p^1\text{-}i interface after hole recombination (which results in the current decay) is complete. The electrostatic effect of this negative charge could then increase the
barrier height and inhibit subsequent conduction. This may be the reason for the current decay observed in the thin i-layer samples. Vardeny has investigated photoluminescence decay in intrinsic a-Si:H and concludes that under these conditions bimolecular diffusion-limited recombination processed with a characteristic time of $10^{-6}$ to $10^{-2}$ seconds can occur(8). Such a time scale is in accord with the observations of the recovery time ($t_r$, §7.2.6), although any comparisons must be treated as highly speculative owing to the uncertainty in what is being measured by the experiment and the relatively complexity of the samples.

In addition to the electrostatic effects associated with the trapped electronic charge, it is also possible that atomic displacements may result, giving rise to a new atomic configuration which persists until the charge is released. The properties of the new configuration could be sufficiently different from the original to inhibit the onset of the current instability under the same external conditions.

As mentioned earlier, experiments on formed devices have shown that once a permanent low resistance state has been established, conduction is localised to an area of order $1\ \mu m^2$. If a similar area is involved in conduction in the case of the current instability, then high peak current densities ($\sim 10^5 \ A cm^{-2}$) and powers ($\sim 10 \ mW$) will occur. The resulting Joule heating may give rise to a high transient local temperature. If the Joule heat is considered as a point source impulse(9), then temperatures of the order of $100K$.

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above ambient could occur for periods of the order of microseconds within the filamentary volume of a-Si:H. Although it is apparent that, in general, such heating effects are insufficient to bring about permanent changes, it is possible that the recovery time corresponds to the time taken for a thermally-excited state to revert to the pre-instability state.

At this point it is appropriate to refer to the results obtained by Pollack on Schottky emission in Pb-Al₂O₃-Pb structures (see §3.3.2 or (10)). Although no instability or switching was reported in this sandwich structure, of particular interest is that a forming process was noted. After forming the current passing through the structure had increased by five orders of magnitude (see figure 3.9). It is suggested that the forming process establishes a positive ionic space charge at the cathode, which increases the effective field and decreases the effective cathode work function. This space charge may originate from migration of Al ions to vacancy nearby interstices in the Al₂O₃ lattice. This argument will be further discussed in §8.3 when the ON-state is considered.

§8.3 ON- and OFF-states

The area dependence experiments reported in §7.3.3 show that for type A devices current flows uniformly through the whole device in the virgin and OFF-states while the ON-state resistance is independent of contact area. For type B devices there are no distinct ON- or OFF-states, and the different nature of types A and
B devices can also be seen from a comparison of the I-V characteristics of the virgin, ON- and OFF-states as described in §7.3.1. A filament is however found in both type A and B devices after forming, and by passing current through the devices in the ON-state it is possible to observe the current path from the changes produced by Joule heating in the reflected colour of a liquid crystal (§7.3.4). The diameter of the filament is estimated to be less than 2µm and this discovery is of major importance in the understanding of the switching mechanism.

If the ON-state resistance was supposed to be thermally activated, i.e.

\[ R \sim \exp \left( \frac{\epsilon}{kT} \right) \]  

(8.7)

then \( \epsilon \) would be much less than \( kT \) in type A devices. Type B devices are more sensitive to temperature than type A. Magnetoresistance measurements (§7.3.5) of the ON-state do not allow any definite conclusions to be reached concerning the amorphous or crystalline nature of the ON-state filament. However, it is probably correct to deduce from the magnetoresistance measurements a longer mean free path than is normally associated in amorphous solids(11). In contrast to the ON-state, the value of \( \epsilon \) in the OFF-state devices was found to be a few tenths of an eV in type A devices but it varied from sample to sample.

From the SEM micrographs it has been established that the "hot spot" (as verified by the liquid crystal technique) is coincident
with changes in the surface morphology of the devices. X-ray microprobe analysis of pore structures, in ON- and OFF-states, with the Cr top (M₄) contact removed, have shown that a Cr signal was located at the filament while no Cr signal was found in the area outside the filament. These results indicate that the ON-state might be associated with a conducting filament containing Cr or Cr-silicide tracks or islands shorting out the i-layer, or even the n-layer.

§8.4 Discussion of possible switching mechanisms

Filamentary conduction has also been observed in single crystal silicon, gallium arsenide, zinc telluride, gallium arsenide phosphide, polycrystalline silicon (see §4.2 and (12)) and amorphous chalcogenide glasses. The reversible memory switching operation in chalcogenide glasses is associated with the growth and destruction of a crystalline filament (7,13,14). It is likely that in the a-Si:H devices, filament formation (not necessary crystalline) is taking place during the forming process but the switching phenomena are clearly very different from those in the chalcogenides, at least operationally. The most obvious difference is the completely nonpolar character of switching in chalcogenide glass devices, in contrast to the marked polarity dependence of the a-Si:H memory switches.

From the X-ray microprobe analysis and the discussion presented in §8.3, it could be argued that the conducting filament consists of
small isolated metallic particles dispersed in a dielectric medium. Extensive work on thin film composite materials (15) has given a great deal of insight into the tunnelling process between isolated metal particles and its dependence on average particle size and separation, applied fields etc. The temperature dependence of the ON-state reported in §7.3.5 is consistent with measurements made on such systems.

It is conceivable that filament formation is induced by the extremely high local field across the M-I-i junction, which may approach $10^6 \text{ V cm}^{-1}$. Under these conditions the tunnelling of field emitted electrons from the top of the electron distribution in the metal electrode becomes the dominant transport mechanism, injecting appreciable electron densities into the semiconductor, as analysed in §8.1 and postulated in §8.2.

The mechanisms underlying the switching phenomena in the a-Si:H devices (i.e. the ON → OFF, OFF → ON transitions) are not well understood at present. Several possible mechanisms are presented below.

§8.4.1 Thermal Model

The thermal models which were used to explain switching in chalcogenide glasses should first be considered as a basis for explaining the a-Si:H switching process. There are however a number of differences between the a-Si:H and the chalcogenide memories.
which suggest that the thermal model is not applicable to the a-Si:H devices:

(i) It has been established that the a-Si:H memories do not form at constant power; in general forming occurs at much lower power ($<10^{-8}$ J) than in the chalcogenides ($10^{-4}$-$10^{-5}$ J)(16)

(ii) The forming, WRITE and ERASE operations for the a-Si:H memories are generally polarity dependent (see Chapter 7 or (16))

(iii) No rise in the temperature of the a-Si:H specimens can be observed immediately prior to switching (see §7.3.4)

(iv) The WRITE and ERASE times are many orders of magnitude faster than those of the chalcogenides, e.g. for the WRITE operation $10^{-8}$s compared with $10^{-3}$s(7).

§8.4.2 Models based on trapped space charge

In many respects the behaviour of the a-Si:H devices appears to be closely related to that of c-Si MISS structures as described in §8.2. The major difference of course is that the c-Si MISS structures are threshold switches whereas a-Si:H MISS structures exhibit non-volatile memory behaviour. It is nevertheless possible that the memory switching in a-Si:H devices may be related to threshold switching in c-Si MISS devices. It was shown in §8.2 that the "forming voltage" derived from the "punch-through" model for c-Si MISS devices does not agree well with experimental data obtained
from the a-Si:H devices. The regenerative switching model which takes into account carrier multiplication mechanism at the "inverted" Si-SiO$_2$ interface (§5.3.2) has quantitatively predicted a number of c-Si MISS properties. For instance, it predicts a threshold independent of $d_n$, which agrees with the observations on c-Si $p^+\cdot n\cdot i$ MISS structures where the n-layer is quite heavily doped, but it is in disagreement with the data from the a-Si:H devices (see §7.2.3).

However from the analyses presented in §8.1, it can be said that in virgin samples with thicker n-layers (i.e. $d_n > n_{\text{nCR}}$), conduction under forward bias is controlled by a process where the injected holes are trapped in deep gap states in the n-layer, followed by a electrode controlled process (e.g. the Schottky effect). This together with the current instability phenomenon reported in §7.2.6, offers a tentative explanation of the static I-V characteristics and the forming process. In some c-Si MISS devices, forming is observed (see §5.2.2) and this process is believed to be caused by a permanent filling of deep traps within the insulator or at the semiconductor surface. The actual processes responsible for the filament formation and subsequent switching operations in a-Si:H devices are not well understood at present. There are many areas which require additional experimental and theoretical work, even in the cases of virgin state conduction and the forming process.
References

(5) Owen, A.E. Private communication.
CHAPTER 9

CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

§9.1 The virgin state

The experimental results presented earlier clearly establish that there is a critical n-layer thickness $d_{nCR}$. For n-layer thicknesses less than $d_{nCR}$ a p$^+$-n-i device behaves like a p$^+$-i structure (i.e. $d_n = 0$). The C-V characteristics of virgin a-Si:H p$^+$-n-i devices in which $d_n < d_{nCR}$ are qualitatively similar to those of an MOS capacitor. The C-V characteristics of p$^+$-n-i structures with $d_n > d_{nCR}$ can be explained by considering the total capacitance to be the sum of three capacitances in series, i.e. the capacitance of the insulator $C_i$, of the surface depletion layer $C_s$ and of the p$^+$-n junction $C_j$. Under reverse bias, the C-V characteristics are similar to those of a reverse biased p-n junction, while the C-V plots in the forward direction show depletion layer capacitance behaviour similar to MIS diodes.

Similarly, the I-V characteristics in the reverse direction are relatively simple and they resemble a reverse biased p-n junction. In the forward direction however the I-V dependence is more complex. Initially there is an ohmic region, followed under certain circumstances, by a region of one carrier space-charge-limited current. The main features which emerge from the SCLC analysis are:
(1) The $I \propto V^2$ regime is only observed when $d_n > d_{nCR}$ in a-Si:H $p^+-n-i$ structures with $10^4$-30-0 vppm doping levels.

(2) The trap density derived from the one-carrier SCLC model for the n-layer ($1.06-4.59 \times 10^{16} \text{cm}^{-3} \text{eV}^{-1}$) is close to the density of gap states reported in the literature ($1.2 \times 10^{17} \text{cm}^{-3} \text{eV}^{-1}$).

(3) The $I \propto V^2$ dependence is absent in $p^+-n-i$ structures with heavily doped (202 vppm) n-layers and thus the one-carrier SCLC model is not applicable in this case.

(4) At higher voltages a trap-filled limit is observed.

(5) At still higher voltages the conduction becomes dominated by a Schottky barrier and this region leads directly into forming.

§9.2 The forming process

It was shown in §7.2.3 that a plot of $V_F$ versus $d_n$ does not pass through the origin. The intercept at $d_n = 0$ is thought to correspond to the breakdown of the reverse biased $n_1-i$ Schottky barrier, and forming occurs when such a voltage is developed in a given $p^+-n-i$ structure. The sequence of events leading up to forming are as follows:

(i) At zero bias the equilibrium currents consist of thermionic emission over the Schottky barrier ($n_1-i$) and a hole diffusion current from the $p^+-n$ junction.
At moderate bias, the thermionic current is aided by a tunnelling current from $W_1$ into the conduction band of the a-Si:H n-layer. The hole current is comparable to the electron tunnel current.

At high biases the electron tunnel current will dominate, and hole injection will increase as a result of a larger forward bias on the $p^+-n$ junction.

Moreover, as discussed in §8.2 unusual current instabilities are observed in $p^+-n-i$ structures where the i-layer is thin ($< 10\text{nm}$), and it is thought that these may be a precursor to forming.

The forming voltage $V_F$ varies linearly with $d_n$ (the n-layer thickness) provided $d_n > d_{nCR}$, but $V_F$ does not scale linearly with $d_i$ (the i-layer thickness). A comparison with theories for crystalline silicon (c-Si) fiSS devices failed to show quantitative agreement in switching voltages.

The experimental results have clearly established that there is a delay time $t_D$ associated with the forming process. There is also some evidence of a correlation between $t_D$ and the onset time of the pre-forming current instabilities mentioned above. The main features relating to these transient phenomena are:

1. The delay time $t_D$ for a-Si:H $p^+-n-i$ structures with $d_n > d_{nCR}$ may be related to the time taken for holes to diffuse through the n-layer.
The $t_D$ and $t_{on}$ versus voltage data show that certain features of models developed for c-Si NiSS devices may be applicable to the a-Si:H structures, although some modifications would be necessary for quantitative development.

The rapid rise in current after $t_{on}$ or $t_D$ has elapsed is considered to be the time needed to build up a critical charge and the critical voltage $V_C$ or $V_{CR}$ is considered to be the minimum voltage needed to build up $Q_C$.

The reduction of $V_C$ or $V_{CR}$ with increasing temperature may occur because at high temperature a smaller forward bias will provide sufficient hole injection to build up $Q_C$.

If a residual electron charge remains trapped close to the $N_i$-i interface after hole recombination, its electrostatic effect may inhibit a second transient current instability in a-Si:H $p^+\!-n\!-i$ structures with thinner i-layers (see §7.2.6 and 8.2).

It is possible that the recovery time ($t_r$) of the transient current instabilities is due to a high (transient) local temperature and $t_r$ corresponds to the time taken for a thermally-excited state to revert to the pre-instability state.

It is also possible that atomic displacements occur during the transient and a new atomic configuration, significantly different from the original, inhibits the onset of a second current instability.
§9.3 ON- and OFF-states and switching mechanisms

A detailed study of the ON- and OFF-states and switching mechanisms were not within the scope of this work but certain observations were made for the sake of completeness. In particular:

(1) After forming a current filament is found in both type A and B devices.

(2) If the ON-state resistance is considered to be thermally activated then the activation energy ($\varepsilon$) is much less than $kT$ in type A devices. In the OFF-state of type A devices $\varepsilon$ was found to be a few tenths of an eV. In type B devices there is almost a continuum of "ON-states", whose activation energies range from $\sim kT$ to a few tenths of an eV.

(3) From its temperature dependence, the ON-state in type B devices might be associated with a conducting filament that is composed of metal islands embedded in the i-layer, and possibly extending into the n-layer.

The mechanisms underlying the switching phenomena in the a-Si:H devices are not well understood at present. Thermal models which have been used to explain switching in chalcogenide glasses are certainly not applicable to the a-Si:H device. It is however possible that in the virgin state the theories developed for c-Si WISS devices can be used to describe the behaviour of the a-Si:H devices, although some modifications must be included to accommodate the amorphous nature of the devices studied in this project.
§9.4 Future work

The discussion presented in §8.1 on virgin devices indicates that additional experimental and theoretical studies of a-Si:H p⁺-n-i devices are required. It certainly would be very useful, following the arguments presented in §8.1, if a model which takes into account the amorphous nature of the devices could be developed from theories of similar crystalline devices. For instance a model which combines the a-Si:H p-n junction and Schottky barrier might predict the I-V and C-V characteristics of the a-Si:H devices obtained experimentally. Another major problem that needs further clarification is the mechanism responsible for the forming process in the low bias, high temperature regime.

It will perhaps throw some light on the forming process if it can explained why type A and B devices exist after forming, as the I-V characteristics of the ON- and OFF-states of these two types of devices are considerably different (see §7.2.5 and 7.3.1).

There is no doubt that filamentary conduction results after forming but the actual mechanism/mechanisms still require further work. As suggested tentatively in §8.3 the ON-state could be a consequence of tunnelling between metallic islands. Detailed measurements of the low temperature conductivity of the ON-states may reveal whether this is occurring.

A more detailed study of the current instability phenomenon observed in the a-Si:H p⁺-n-i structures may provide another area
Where possible mechanisms/mechanisms for forming may be ascertained. Finally, the following experiments are suggested to provide additional information which should improve our understanding of the virgin state conduction, the forming process and the switching operation of the a-Si:H devices:

1. To fabricate a-Si:H devices with metal (e.g. Cr) deposited "in-situ" in the i- and/or n-layer; this may give some insight in the tunnelling process mentioned above.

2. A third ohmic contact can be made to the n-layer (as in 3-terminal c-Si NiSS devices) and this will provide:
   a. Some indication of the potential distribution between the n-i contact and the n-layer.
   b. A means of injecting or extracting charge (holes in p^+-n-i structure; electrons in n^+-n-i configuration) from the n-layer and the n-i interface. This can provide basic information which is unobtainable in a two-terminal device, and may also prove useful as a practical device.
APPENDIX

PUBLISHED WORK AND PATENTS


Electronic Switching in Amorphous Silicon Junction Devices

P. G. LeComber  
Carnegie Laboratory of Physics  
University of Dundee  
Dundee, Scotland

A. E. Owen  
Department of Electrical Engineering  
University of Edinburgh  
Edinburgh, Scotland

W. E. Spear  
Carnegie Laboratory of Physics  
University of Dundee  
Dundee, Scotland

J. Hajo  
Department of Electrical Engineering  
University of Edinburgh  
Edinburgh, Scotland

W. K. Choi  
Department of Electrical Engineering  
University of Edinburgh  
Edinburgh, Scotland

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Electronic switches are solid-state devices that can be changed from a nonconducting OFF state to a conducting ON state by an appropriate electrical signal. The importance of such devices in the development of solid-state digital electronics has been enormous and is likely to remain so in the foreseeable future, especially with the increasing demand for memory elements.

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The present article is concerned with two-terminal switching devices. Generally, these have one or the other of the two types of current-voltage \((I-V)\) characteristics shown schematically in Fig. 1a, b. In Fig. 1a the device switches from its OFF to its ON state at a critical threshold voltage \(V_{th}\), but if the ON state conditions fall below a critical holding point \((I_h, V_h)\), the device reverts spontaneously to its OFF state. Devices of this kind are called threshold switches; they are nonpermanent, or "volatile," and they always revert to the OFF state in the absence of an appropriate bias. In Fig. 1b there is again a critical switching voltage for the OFF to ON transition, but both ON- and OFF-state characteristics extrapolate through the \(I-V\) origin. Devices of this kind are therefore permanent, or nonvolatile, and they are called memory switches. Memory devices can remain in either the ON or OFF state more or less indefinitely, whether or not a bias is applied and the ON to OFF transition is usually triggered by a current pulse.

By the early 1970s many examples of threshold and memory switching had been reported in homogeneous thin films of a variety of amorphous materials, including simple oxides, transition-metal oxides, elemental selenium, and boron. By far the most important materials, however, were the chalcogenide glasses in which, depending on composition, reproducible characteristics of the kind illustrated in Fig. 1a (threshold switching) or Fig. 1b (memory switching) may be obtained (Ovshinsky, 1968; Owen and Robertson, 1973). A substantial specialist literature on electrical switching

![Fig. 1. Current-voltage characteristics for (a) threshold switching and (b) memory switching.](image-url)
in the chalcogenide glasses has developed, and although there are still some controversial features, generally accepted models of at least a semiquantitative kind are now reasonably well established for both types of switching (Adler et al., 1978; Owen et al., 1979).

This article is concerned with recent studies of a rather different switching behavior in heterogeneous structures of amorphous hydrogenated silicon, which evolved from a collaborative project between the authors' groups at the Universities of Dundee and Edinburgh in the United Kingdom. A preliminary account of the work has already been published (Owen et al., 1982), and in the following sections a more detailed description of the experimental observations will be presented.

Before proceeding, however, it is worth noting that, by contrast with the chalcogenide glasses and despite the almost unprecedented growth in research and development on amorphous silicon (a-Si) since the mid-1970s, very little has been reported on electrical switching in the latter material. To put the recent observations in context it is pertinent therefore to review briefly the relatively few previous reports of switching in a-Si.

III. Previous Work on Electrical Switching in Amorphous Silicon

Some cursory observations of threshold switching in homogeneous films of a-Si, with very tentative evidence for memory behavior, were described by Feldman and Moorjani (1970) and Moorjani and Feldman (1970) contemporaneously with some of the early literature switching in chalcogenide glasses. More detailed experiments on the same structures were reported later (Feldman and Charles, 1974; Charles and Feldman, 1975). The authors studied vacuum-evaporated films of a-Si in the range 0.3–2.0 μm thick, fitted with titanium electrodes. They also, incidentally, made similar observations on evaporated films of germanium, boron, and boron plus carbon. As threshold switches these a-Si structures had threshold voltages $V_{th}$ of 5–10 V, OFF resistances in the range 1–30 kΩ, and an ON resistance of about 100 Ω. In common with the chalcogenide glasses, there was a delay time before switching of 20–50 μsec or more (at room temperature) and the actual switching time was at least several microseconds. Feldman et al. did not, however, report any initial "forming" process, unlike the situation in chalcogenide glass switches (see also Part V). As already noted, there was some tentative indication of memory switching, but that feature was apparently not substantiated. Feldman and Charles (1974) interpreted the results in terms of a simple and qualitative electrothermal model involving the formation of a conducting filament; a similar, more quantitative model has been developed for switching in chalcogenide glasses (Owen et al., 1979).

The work of Feldman and his colleagues, which originated in the early
1970s, seems to be the only investigation of switching in a-Si until the later studies of Dey and Fong (1977, 1979) and Dey (1980). These authors report results very similar to those of Feldman et al. They studied thin films of a-Si in the range 0.3–1.5 μm thick, deposited by electron-beam heating in a vacuum evaporator. Titanium contacts were again used, either in the form of evaporated films or as probes. Dey and Fong reported only threshold switching, with \( I-V \) characteristics similar to those in Fig. 1a; they did not mention any evidence for memory behavior. In contrast to Feldman et al., however, Dey and Fong did observe forming effects; that is, the initial threshold voltage was relatively large but it decreased to a more or less constant value after a number of switching cycles. In Dey and Fong’s devices the threshold voltage varied systematically from about 6 V for the thinner films (≈0.3 μm) to about 9 V for the thicker films (≈1.2 μm). The delay time before switching was in the range 2–60 μsec, varying in a systematic way with pulse height, pulse duration, and repetition rate, again in a manner very similar to switching in calcogenide glasses (Adler et al., 1978; Owen et al., 1979). Dey and Fong also interpreted their results in terms of a simple one-dimensional electrothermal model, but one developed a little more quantitatively than that by Feldman et al.

It should be noted that both Feldman et al. and Dey and Fong used a-Si films deposited by vacuum evaporation. This probably accounts for the relatively low OFF-state resistances which they both found (100–100 kΩ). It is now well established that vacuum-evaporated a-Si is a very different material from the hydrogenated form of a-Si obtained, for example, by the carefully controlled glow-discharge decomposition of silane (e.g., Spear, 1977).

Three papers concerned specifically with switching in hydrogenated amorphous silicon by Gabriel and Adler (1982), den Boer (1982), and Owen et al. (1982) appeared almost concurrently early in 1982, each reporting very different effects observed in different a-Si structures. Our own work (Owen et al., 1982), including recent results, is described in detail in the following sections.

Den Boer studied \( n^+ - i - n^+ \) structures of a-Si prepared by the glow-discharge decomposition of SiH₄ ("i" stands for "intrinsic" or undoped material). The \( n^+ \) layers were 50 nm thick and prepared by adding 1% PH₃ to the SiH₄ gas flow; the \( i \) layer in different devices ranged in thickness from 2.5 to 5 μm. Den Boer found that the \( n^+ - i - n^+ \) devices functioned as threshold switching devices with nonpolar characteristics similar to those sketched in Fig. 1a. For the first switching cycle the threshold voltage was in the range 40–100 V, but for all subsequent operations it was only 10–35 V, depending on the \( i \) layer thickness (as the \( i \) layer thickness increased the threshold voltage also increased). The OFF-state resistance of the \( n^+ - i - n^+ \) switches
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was about 1 MΩ, and the ON-state resistance about 1 kΩ. There was again an observable delay time before switching, ranging from a few microseconds when the applied voltage was about 3 V greater than $V_T$ to about a millisecond for voltages within 1 V of $V_T$. The $n^+ - i - n^+$ threshold switches could be cycled through at least $10^9$ stable switching operations. Den Boer also compared structures with chromium or a combination of chromium and $n^+$ contacts (i.e., Cr-$n^+ - i - Cr$ and Cr-$i - Cr$). The former had rectifying characteristics while the latter switched but were very unstable.

Gabriel and Adler (1982) prepared their a-Si films by sputtering from a polycrystalline silicon target in an argon-hydrogen plasma. In all cases their devices were notionally homogeneous thin films of intrinsic a-Si:H with molybdenum contacts. The samples were fabricated under a wide range of deposition conditions in two sputtering systems, and although results from some of the devices were rendered rather doubtful because of contamination problems, in no case did Gabriel and Adler observe any evidence of reversible switching. They concluded that, in contrast to the chalcogenide glasses, a-Si does not have the electronic and structural properties required for reversible switching.

III. Device Structure and Fabrication

We turn now to the work on electronic switching carried out in the authors' laboratories. Although a number of different a-Si multilayer structures have been investigated, all the results discussed in the following refer to $p^+ - n - i$ devices deposited in this sequence by the glow-discharge technique, with gas-phase doping. Stainless steel substrates were generally used and the total thickness of the deposited a-Si layers was between 0.5 and 1.0 μm. After completion of the a-Si deposition a series of gold (Au), aluminum (Al), or nichrome (NiCr) dots (up to approximately 1 mm in diameter) was evaporated onto the surface of the samples, and the top contact was completed either by a probe or by a thin wire attached to the metal dots with conducting silver paste.

IV. Static Current-Voltage Characteristics of Virgin Devices

Typical current-voltage ($I-V$) characteristics for a freshly prepared (unswitched) device are illustrated in Fig. 2a in both the forward and reverse directions. (The forward direction is defined such that the substrate, and hence the $p^+$ region, is positively biased.) It must be emphasized here that these measurements were taken "by hand," point by point, in a manner that required a few seconds for each point to be measured. (The significance of
In the forward direction there is a region of ohmic behavior over a limited voltage range followed by an abrupt change to a markedly nonohmic region until, at the point indicated by the arrow, the device is unstable and it is impossible to continue with point-by-point measurements. The change from ohmic to nonohmic behavior is more clearly apparent in the effective conductivity versus applied voltage plot of Fig. 2b. As the ambient temperature increases, the onset of nonohmic behavior moves to lower voltages. In the reverse direction, corresponding to a negative potential applied to the $p^+$ side, there is an initial ohmic region which is symmetrical for positive and negative voltages. However, the change to nonohmic behavior is much more gradual in the reverse direction, leading to the eventual breakdown of the device.
As noted in the previous section, during point-by-point measurements under forward bias, the a-Si $p^+-n-i$ device tends to become unstable when the applied bias is about 24 V at room temperature. At higher temperatures the instability occurs at lower voltages, as indicated by the arrows in Fig. 2a. On attempting to increase the voltage still further, the device switches into a low-resistance ON state. Typical $I-V$ characteristics for both polarities in the ON state are shown in Fig. 3; the $I-V$ curve is ohmic, it extrapolates through the origin (i.e., the ON state is permanent), and it is slightly asymmetrical. Note that the current is now measured in milliamperes and that the voltages across the device are small. On increasing the voltage in the forward direction the ON state current continues to increase apparently indefinitely, subject only to any current-limiting resistor, and the device is eventually destroyed, presumably by Joule heating. In the reverse direction, however, another instability is observed, and at about $-1$ V (typically) the

![Graph](image)

**Fig. 3.** Current-voltage characteristics of a device in the ON state, at different temperatures, in the forward and reverse directions. The forward direction corresponds to $p^+$ layer positively biased. (○) forward bias, 80°C; (△) reverse bias, 80°C; (□) reverse bias, 30°C.
device switches back into a high-resistance OFF state. The OFF-ON transition may now be repeated by biasing in the forward direction, but on the second and all subsequent switching operations the forward threshold voltage $V_{T_{HF}}$ occurs at a much lower voltage than the first operation, e.g., at $\approx 5\, \text{V}$ compared with the $25\, \text{V}$ observed under the conditions obtaining for the measurements shown in Fig. 2. The first OFF-ON transition, occurring at a relatively high voltage, seems therefore to be unique and by analogy with the usage of switching in chalcogenide glasses, it is referred to as "forming."

The formed a-Si $p^+-n-i$ device may be cycled through ON and OFF states by a sequence of biasing in forward and reverse directions with critical points at $V_{T_{HF}}$ and, in the reverse direction, $V_{T_{HR}}$. A complete and typical characteristic obtained on a curve tracer is illustrated in Fig. 4. On occasions the device appears to go through a number of intermediate ON states during the OFF-ON transition, and this is indicated in the figure. In addition, there is often an observable and appreciable region of negative resistance in the reverse-biased OFF state characteristic of a formed device, denoted by $N$ in Fig. 4.

VI. Formation: Dynamic Characteristics

The forming process (i.e., the first OFF-ON transition) does not occur instantaneously when a voltage step or pulse is applied to the a-Si $p^+-n-i$ device. Initially there is a delay time $t_D$ during which the device current remains essentially constant at the OFF-state value appropriate to the voltage across the device. Only after this delay does the current begin to increase, and it then rises almost instantaneously to its ON-state value. The forming delay time is an extremely sensitive function of the applied forming

![Fig. 4. Complete static current-voltage characteristics of a formed a-Si $p^+-n-i$ device, showing the forward and reverse threshold voltages, $V_{T_{HF}}$ and $V_{T_{HR}}$, respectively.](image-url)
voltage $V_f$, and typical data, obtained at three temperatures, are given in Fig. 5. The forming delay time varies over nearly 10 orders of magnitude, from a few hundred seconds at low forming voltages to about 10 nsec at high $V_f$. In particular, at a temperature-dependent critical forming voltage $V_{cr}$ there occurs virtually a discontinuous change in $t_D$. The forming voltages $V_{cr}$ indicated in Fig. 5 are approximately the same as the voltages at the points of instability marked by the arrows in Fig. 2a; $V_{cr}$ also corresponds to the forming voltage obtained in experiment with a curve tracer, operated in ac mode at a frequency of 50 Hz. It can also be seen in Fig. 5 that above and below $V_{cr}$ the delay time tends to a value that seems to be approximately independent of both voltage and temperature; for the particular results illustrated, $t_D$ is in the range $10^2 - 10^3$ sec for $V < V_{cr}$ and lies between 10 and 100 nsec for $V > V_{cr}$.

The results plotted in Fig. 5 for $V < V_{cr}$ correspond of course to voltages less than the point of instability indicated in Fig. 2a. There does appear to be a lower limit to the forming voltage, however, and present results indicate that the limiting voltage coincides with the bias at which the $I-V$ characteristics change from their ohmic to nonohmic behavior (see Fig. 2b). Several

![Fig. 5. The delay time for forming $t_D$ as a function of applied forming voltage at three different temperatures: (○) 30°C, (◇) 80°C, (+) 160°C.](image)
experiments have shown that virgin devices fail to switch (form) even if held for many hours at a forward bias only just below the nonohmic region. In other words, forming occurs at any forward bias within the nonohmic region of the $I-V$ characteristics, but at voltages below the point of instability $V_D$ is comparatively long. It must also be emphasized again that the device current remains constant at its OFF-state magnitude during the delay time, even when $t_D$ is 100 sec or more.

Preliminary experiments have been carried out to determine the effects of device geometry on the forming voltage $V_F$. It was found that $V_F$ increases linearly with the thickness $d_n$ of the $n$ layer. Data for typical $p^+ - n - i$ devices are plotted in Fig. 6. In this case $V_F$ was measured by applying a voltage ramp and its value coincides with the voltage $V_{cn}$ indicated in Fig. 5. It can be seen that the results do not extrapolate to zero voltage for zero $n$ layer thickness.

The charge $Q = \int_0^t I dt$, which flows through or into the device during the forming delay time, has been determined for $V_F > V_{cn}$. Figure 7 shows that in this range of $V_F$ the ratio $Q/d_n$ is approximately independent of $V_F$ and $d_n$ for $n$ layer thicknesses between 215 and 780 nm. This could mean that forming occurs when a critical volume charge has accumulated in the $n$ region.

VIII. Dynamic Switching of Formed Devices

The principal experimental features of the pulsed operation of formed a-Si $p^+ - n - i$ devices have already been described by Owen et al. (1982). A representative diagram drawn from an oscilloscope trace of the OFF $\rightarrow$ ON
The ratio of charge to layer thickness \((Q/d)\) as a function of forming potential. 

d, 215 am ( ), 654 am (O), 780 am ( ).

transition on applying a fast voltage ramp is shown in Fig. 7. The main points to note are as follows:

(i) When biased with a pulse in the forward direction, the device switches ON, provided the pulse height exceeds the static threshold voltage \(V_{TH}\) as defined in Fig. 4.

(ii) On the time scale of \(-1\) nsec or less, there is no observable delay time in the response of a formed device. The device current follows the applied voltage instantaneously on this time scale.

(iii) Provided the pulse is long enough, the ON state is permanent and the pulse duration required for switching to a memory state increases as the

Fig. 7. The ratio of charge to layer thickness \((Q/d)\) as a function of forming potential.

Fig. 8. The OFF-ON switching transient of a formed device, drawn from an oscilloscope trace: (a) applied bias, vertical scale: 2 V per division, horizontal scale: 20 nsec per division; (b) device current, vertical scale: approximately 6 mA per division, horizontal scale: 20 nsec per division.
pulse height decreases toward $V_{\text{thr}}$. In typical cases a permanent ON state is obtained with pulse durations of a few tens of nanoseconds and magnitude $\sim 5\, \text{V}$ in excess of $V_{\text{thr}}$.

(iv) Similarly, on biasing in the reverse direction with a pulse of height $> V_{\text{thr}}$, the device switches from ON $\rightarrow$ OFF and again there is no observable delay in response.

(v) The ON-state appears to be truly permanent. No detectable changes have been observed in devices stored in their ON state for a year or more.

VIII. Discussion of Possible Switching Mechanisms

The mechanisms underlying the switching phenomena in the a-Si devices are not understood at present; clearly, more data will be required to explain these exceptional properties. In the following we therefore draw some comparisons with other related switching devices and only briefly speculate on possible mechanisms.

Although there is no observation of memory switching in analogous crystalline Si (c-Si) devices, threshold switching is well known in c-Si $p^+ - n$-$i$, $n^+ - p$-$i$, and related structures (Yamamoto and Morimoto 1972, Yamamoto et al., 1976; Buxo et al., 1978; Sarrabayrouse et al., 1980; Simmons and El-Badry, 1978; Kroger and Wegener, 1973, 1975). The $i$-layer in these devices is usually a SiO$_2$ film ($\leq 40\, \text{Å}$), thin enough to pass appreciable tunneling currents, but it may be significant that these metal-insulator-semiconductor-semiconductor (MISS) devices can also be fabricated in an "all-Si" form using polycrystalline Si as the $i$-layer (Kroger and Wegener, 1975). These devices switch to a nonpermanent ON state when the $p^+ - n$ (or $n^+ - p$) junction is forward biased, which is the same polarity producing the memory ON state in the a-Si structures. In the MISS device the switching action is associated with minority-carrier injection from the $p$-$n$ junction and accumulation at the interface of the $i$ layer, normally leading to punchthrough to the injecting contact, which causes the device to switch ON. The values of the threshold voltage are similar to those observed in the a-Si forming process, and it is conceivable that for this operation the processes are similar. The experimental results described in Part VII, which suggest that the forming process is likely to be charge controlled, would not be inconsistent with this model.

For the c-Si MISS $p^+ - n - i$ threshold device the values of threshold voltage are predicted (Simmons and El-Badry, 1978) to depend on $(d_n - W)^2$, where $d_n$ is the thickness of the $n$ layer and $W$ is the width of the depletion region, and for low donor concentrations this dependence is supported experimentally. In contrast, the results in Fig. 6 show that in the a-Si devices the forming voltage varies linearly with $d_n$. It is difficult to decide at present
whether this disagreement suggests a different mechanism or whether it arises from our attempt to extrapolate from a model developed for a crystalline threshold device to an amorphous memory junction.

An alternative model, based on a regenerative process, has also been suggested for the c-Si MISS devices (Sarrabayrouse et al., 1980), taking into account a carrier multiplication mechanism at the "inverted" Si–SiO₂ interface. The model correctly accounts for a number of MISS properties; for example, it predicts a threshold independent of $d_n$, which agrees with the observations on $p^+–n−i$ MISS structures when the $n$ layer is more heavily doped. But this model is also in disagreement with the data for the a-Si devices shown in Fig. 6, and just as for the "punchthrough" model, it is therefore difficult at the present stage to decide whether the regenerative model could be relevant to the understanding of a-Si memory switching.

In the field of amorphous semiconductors much attention has been given over the past 10–15 years to memory switching devices fabricated from multicomponent chalcogenide glasses in which the reversible memory action is associated with the growth and destruction of a crystalline filament (Ovshinsky, 1968; Cohen et al., 1972; Steventon, 1974; Owen and Robertson, 1973; Owen et al., 1979). Although it is very likely that in the a-Si devices some form of filament formation (not necessarily crystalline) is taking place in the OFF–ON transition, the switching phenomena are clearly very different from those in the chalcogenides, at least operationally. The most obvious difference is the completely nonpolar character of switching in chalcogenide glass devices, in contrast to the marked polarity dependence of the a-Si memory switches. More important, perhaps, the switching and setting times for the a-Si device are much faster (~10 nsec for either the OFF–ON or ON–OFF transition, compared with at least several milliseconds in chalcogenide devices) and the energy involved in the switching process is considerably lower (1 μJ or less, compared with 1 mJ or more). Also chalcogenide glass devices require voltage pulses of magnitude 25–30 V (for a device ~1 μm thick) to establish the ON state, and very often they need 100 or more "forming" cycles before reasonably stable operation is achieved. This again contrasts with the operation of the a-Si memory switch, in which (for a total device thickness of ~1 μm) there is a single forming step with a threshold voltage of about 30 V, and for all subsequent operations the forward threshold ($V_{th}$) is 4–6 V.

The closest parallel to the a-Si devices described in this paper seems to be the observation of memory switching in heterojunctions of n-type ZnSe grown epitaxially on p-type (single-crystal) Ge substrates, reported by Hovel (1970) and by Hovel and Urgell (1971). The ZnSe–Ge heterojunction devices are polar and the transition times for the OFF–ON and ON–OFF operation are both in the region of 100 nsec or less. Similar, but not so
well-substantiated, memory switching characteristics have also been briefly reported in devices fabricated by forming Schottky contacts on n-type GaAs and Si (single crystal) (Moser, 1972). Hovel and Urgell (1971), have tentatively and qualitatively explained switching in the heterojunction by a model involving the filling and emptying of traps in the ZnSe, with the formation of a current filament in the ON state. However, even in this case of superficially similar characteristics, there are notable differences. Most significantly, the polarity required for switching in the ZnSe–Ge heterojunction is the opposite to that found in the a-Si devices, and the OFF–ON threshold voltage for the ZnSe–Ge switch decreases substantially with temperature (from about 1 V at 260 °K to less than 0.1 V at 800 °K), whereas V for the a-Si devices investigated so far is at the most only weakly temperature dependent. In addition, the memory state of the ZnSe–Ge heterojunctions is generally lost within a few weeks, whereas no change in the characteristics of the a-Si memory devices has been observed after storage over a period of 18 months.

To conclude this chapter it is perhaps worthwhile to note that the switching phenomena observed in the a-Si memories are not the only nanosecond processes known for this material. Drift mobility studies, which show that electron transit times across about 1-μm-thick films are of the order of 10 nsec or so, have been known for over a decade (LeComber and Spear, 1970; Spear, 1983). More recently, it has been demonstrated that hydrogenated amorphous silicon can be used to modulate light at subnanosecond speeds (Phelan et al., 1981; see also Chapter 13 by Phelan of this volume). In pulsed laser annealing of a-Si it has been suggested that the electron–hole plasma generated by the laser could produce rapid second-order phase transitions (van Vechten et al., 1979). The challenge and excitement in understanding the a-Si memories lies in discovering whether the origins of the fast switching processes are electronic, structural, or both.

ACKNOWLEDGMENT

The authors are grateful to the Venture Research Unit of British Petroleum International PLC for a grant supporting the research described in this paper.

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15. ELECTRONIC SWITCHING IN a-Si JUNCTION DEVICES


THE SWITCHING MECHANISM IN AMORPHOUS SILICON JUNCTIONS


* Carnegie Laboratory of Physics, University of Dundee, Scotland.
* Department of Electrical Engineering, University of Edinburgh, Scotland.

Extensive new results have been obtained on memory switching in a-Si.p+n junctions. It is shown that the ON-state has its origins in a highly conducting filament less than 1 μm in diameter. The physical mechanisms that could play a role in the switching operations are discussed.

1. INTRODUCTION

Threshold and memory switching in the chalcogenide glasses greatly stimulated research on these materials in the late 1960s and early 1970s 1, 2. In spite of the wide-ranging work on amorphous Si (a-Si) in recent years, memory switching phenomena were not observed and this led to a general belief that homogeneous films of this and other tetrahedrally bonded amorphous materials do not possess the physical properties required for switching behaviour 3. However, some three years ago we demonstrated that heterogeneous junction layers of a-Si could be made to exhibit reliable, fast, polarity dependent memory switching 4-6. The present paper is concerned with recent results on these specimens.

As prepared, the a-Si layers, generally with a p+n structure, require one forming operation after which they are in a non-volatile low resistance ON-state. They can be switched back (ERASED) to a non-volatile high resistance OFF-state by the application of a negative potential to the p layer and switched ON again (WRITE operation) by a positive voltage. This cycle can be repeated many times 5, 6. The particular exciting aspect of these devices is their remarkable switching speed. Pulses of a few volts in height and a few tens of nsecs duration 5, 6 are sufficient for both the WRITE and ERASE operations.

In the first part of this paper our latest results, mainly for formed devices, will be presented. This will be followed by a discussion of possible physical mechanisms that could be playing a role in the switching operation.

2. SPECIMEN PREPARATION

The samples were prepared by the RF glow discharge decomposition of silane or appropriate silane gas mixtures. The majority of the results have been obtained on specimens having a p+n structure where i denotes an undoped layer. We have also observed similar results for n+p'i and related structures and recently

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(North-Holland Physics Publishing Division)
Gangopadhyay et al. have reported memory switching in p^i^n^i^ samples. The samples were deposited onto Corning 7059 glass substrates at 300°C and generally prepared with Cr bottom electrodes and Al or Cr top contacts, although a number of other metals have been investigated. The active area of the samples, defined by photolithographic techniques, ranged from about $10^{-7}$ cm$^2$ to $10^{-3}$ cm$^2$. The work has also been extended to specimens in which the a-Si i-layer was replaced by an insulator. The results for these samples showed the same general features as those reported for the p^i^n^i^ layers and will be described in subsequent publications.

3. STATIC EXPERIMENTAL RESULTS

A number of dc experiments have been carried out on formed devices in an attempt to provide additional information primarily about the nature of the ON-state. The current-voltage characteristics of recent p^i^n^i^ specimens had the same general features as those reported previously, although by carefully controlling the forming process their ON-state resistances were generally kept at a somewhat higher level (~1kΩ).

3.1. Area Dependence of ON- and OFF-state Resistances

Fig. 1 shows the area dependence of the OFF-state resistance, $R_{OFF}$, for samples of different area fabricated from a single p^i^n^i^ deposition run. These results were obtained on specimens that had been previously switched many times. Within the experimental scatter, $R_{OFF}$ clearly scales with the reciprocal of the area $A$ demonstrating that in the OFF-state the current flows throughout the whole area of the specimen.
In complete contrast, the values of the ON-state resistances, $R_{ON}$, for the same specimens show no area dependence at all as can be seen from fig. 2. This result can be understood only if the ON-state has its origin in a highly conducting filament, less than a few μm in diameter, that extends at least part of the way through the specimen thickness. This result, although not entirely unexpected, will obviously be of central importance in developing a model for the switching process. A direct proof of the existence of a filamentary ON-state is provided by the results in section 4.

3.2. Temperature Dependence of the ON- and OFF-states

The temperature dependence of both the ON- and OFF-state conductance has been measured over the temperature range from about 230K to 400K. Results for a typical p+n specimen are shown in fig. 3. The OFF-state conductance $G_{OFF}$ varied slowly with temperature, increasing by less than a factor of three between 230K and 360K. The ON-state conductance was even less temperature dependent, increasing by only 10% over this temperature range. The insensitivity of these device parameters to temperature is also observed in other properties. For example, the magnitudes of the WRITE and the ERASE voltage, measured under pulsed conditions, both increase by only a factor of 2.5 as the temperature is decreased from 400K to 200K. Clearly the general insensitivity of the switching parameters must also be a feature of any model proposed to explain the switching behaviour.

3.3. Magnetoresistance Measurements of the ON-state

Transverse magnetoresistance measurements of the ON-state of a number of specimens have been carried out at room temperature up to fields of 0.5T. Within the experimental error, $\Delta \rho/\rho$ was proportional to $B^2$ and found to be positive. The values of $\Delta \rho/\rhoB^2$ ranged from $(0.5 \text{ to } 2.0) \times 10^{-4} \text{T}^{-2}$. Experiments on phosphorus doped a-Si after thermal crystallisation also gave a positive magnetoresistance with the same $\Delta \rho/\rhoB^2$ dependence. Unfortunately, no results on homogeneous undoped glow discharge a-Si films have been reported.

It is therefore difficult to draw any definite conclusions about the amorphous or crystalline...
nature of the ON-state filament from the present results. However, it is probably correct to associate the $B^2$ dependence of the memory ON-state with a longer mean free path than is normal in amorphous solids. Using conventional crystalline theory the magnitude of the measured $\frac{\Delta\tau}{\tau_{\text{Bulk}}}$ would lead to an effective mobility $\sim 100\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ in support of this suggestion.

4. OBSERVATION OF ON-STATE FILAMENT

In order to learn more about the ON-state a series of experiments have been carried out in which the surface of the a-Si device was covered with a thin layer of thermochromic liquid crystal. By passing current through the device in the ON-state it is possible to observe the current path from the changes produced by Joule heating in the reflected colour of the liquid crystal (LC). The results for two 20μm diameter structures, viewed through a high power optical microscope, are given in fig. 4. Fig. 4(a) shows the LC surface in the absence of any current flow through the specimen and fig. 4(b) shows a sample with current flowing in the ON-state. The change in the LC appearance produced by Joule heating within the filament can be clearly seen. Fig. 4(c) represents another device in which the filament has been made more visible by passing a larger current through it. We estimate from a number of measurements that the ON-state is associated with a filament of maximum diameter 0.5μm. The result therefore has interesting implications for the understanding of the switching process. The visual observation of the current filament has also enabled us to establish that switching a device OFF and ON again produces the current filament in the same place and this implies that the switching processes are not destructive.

In another series of experiments the specimens were covered by a thin layer of a liquid crystal, 4-cyano-4 allylbiphenyl, which undergoes a nematic-liquid phase transition at 35.3°C. The phase boundary may be observed quite easily in cross-polarised light and the transition was found to be fast and without

![FIGURE 4](image.png)

Photographs of LC surface covering 20μm diameter memories. The arrows in (b) and (c) denote the positions of the current filaments.
hysteresis. If the sample temperature is fixed using a thermostatically controlled stage, the difference in temperature between a region of local heating at a temperature $T_h$ and the surrounding film (at $T_f$) may be determined. The results indicate that no observable temperature rise occurred as a result of applying electrical power to the pore in either the unformed stage just prior to forming, or in the formed OFF-state just prior to switching. However, as described above, in the ON-state local heating which results on applying continuous power could be clearly seen. The effect of changing the RMS power applied to a 50μm diameter pore was studied using a continuous train of 300ns pulses. The stage was maintained at 21°C, thus the phase boundary represented the locus of points $(35.3-21) = 14.3°C$ above the film temperature. These isotherms were circular and in the particular case studied were symmetric about the centre of the pore.

A plot of the phase boundary diameter $d_i$ vs. RMS power $P$ is shown in fig. 5. Although there is considerable scatter it can be seen that the relationship between $d_i$ and $P$ is substantially linear for $d_i \geq 2μm$. Below this the accuracy of the measurements is limited by the resolution of the microscope used. A linear dependence of $d_i$ on $P$ is obtained as a solution of the heat conductivity equation for an idealised system of this kind, in which the source of local heating is assumed to be much smaller than $d_i$. Thus this data indicates that the diameter of the ON-state filament must be much less than 2μm, in agreement with the above experiments.

5. DYNAMIC BEHAVIOUR

In an earlier publication the existence of a voltage dependent delay time had been established for the forming operation. In the course of our recent work we have observed a number of other time dependent effects and these will be described in the following.

5.1. Current Instabilities in Unformed Structures

Current instability phenomena have been observed at voltages below those required for forming, in unformed a-Si p'n' structures with thin i-layers. Typical results obtained under pulsed operation are shown in fig. 6 for three pulse heights decreasing in amplitude from (i) to (iii).
It can be seen that the current increases after a delay time such as $\tau_{ij}$. At first sight the results in fig. 6(a) for the unformed a-Si memories appear to be similar to those observed in crystalline Si MISS devices. However, the a-Si p-n device does not remain in a high conductivity state whilst the voltage is maintained, as is the case for the MISS. The current increases fairly rapidly and then decays over a somewhat longer time-scale, resulting in an asymmetric current pulse as shown in fig. 6(b). However, it is worth emphasising that these current instabilities were observed at voltages just below those required for forming. If the voltage pulse was left on for many tens of microseconds then, some time after the first, a second current pulse would propagate through the sample, and then a third, etc. As the applied voltage $V$ approached the forming voltage $V_F$ these current pulses appeared to merge until at $V = V_F$ the current level remained high as the device formed. These current instabilities therefore appear to be an important precursor to the forming process.

5.2. WRITE and ERASE Delay Times

We have recently observed a delay in the WRITE operation which is a strong function of the WRITE pulse magnitude as shown in fig. 7. Note that these delay times $t_d$ are significantly faster than the forming delay times reported previously.6 If the results in fig. 7 are expressed in the form $t_d = t_o \exp(-V/V_0)$ then $t_o = 335$ns and $V_0 = 4.5$V. Similar results have been obtained for all the specimens investigated although the $V_o$ values ranged from about 0.5V to 13V.
Experiments to measure any ERASE delay time were unsuccessful implying that any delay was less than the rise time of the measuring circuit, i.e. typically less than 5 ns.

6. DISCUSSION OF POSSIBLE SWITCHING MECHANISMS

The work described above contained a number of important new results. Probably the most crucial of these to an understanding of the physical processes underlying the switching mechanism, was the proof of the existence of a filament in the memory ON-state. Filamentary conduction has been observed previously in a wide range of materials. These include single crystal silicon, gallium arsenide, zinc telluride, gallium arsenide phosphide and polycrystalline silicon, all of which can show current-voltage characteristics associated with threshold switching. This applies as well to the amorphous chalcogenide glasses in which both threshold and memory behaviour can be observed. In the following we shall begin by discussing the filament formation and then describe some of the models that have been used for these materials and discuss their relevance to the switching in a-Si.

6.1. Filament formation

During the forming process which, as has been demonstrated, leads to a current filament, the metal-insulator barrier of the device will be under reverse bias. This suggests that the forming is likely to be associated with extremely high local fields across the thin a-Si i-layer which may approach $10^6 \text{Vcm}^{-1}$. Under these conditions tunnelling of field emitted electrons from the top of the electron distribution in the metal electrode becomes the dominant transport mechanism, injecting appreciable electron densities into the semiconductor. The current instabilities described in section 5.1 would certainly be consistent with such a model.

How is the reproducible filament produced during the forming process? A possible answer is suggested by the extensive work on thin film composite
Materials in which small isolated metallic particles are dispersed in a dielectric medium. This work has given a great deal of insight into the tunneling process between isolated metal particles and its dependence on average particle size and separation, applied fields, etc. It is feasible that the high fields and current densities developing locally during forming could lead to enhanced diffusion of metallic particles from the electrode into the thin insulator. Such a region would become the preferred current path carrying the electron current in the ON-state. Further experimental work is required to confirm such a model; the observed field and temperature dependence in the ON-state is certainly consistent with results established in the previous work on these systems.

6.2. Possible Mechanisms for Memory Switching

The above considerations refer to the initial formation of the filament but cannot as such explain the subsequent memory switching. We should now like to critically discuss a number of possible mechanisms to explain this behaviour.

6.2.1. Thermal models

At first sight, this model, used to explain the behaviour of the amorphous chalcogenide memories, might appear to offer a basis for explaining the a-Si switching processes. In the chalcogenides the ON-state is associated with a filament of crystalline material which is formed after sufficient power has been applied to the layer to melt a small area of the material. Switching OFF is achieved by burning out this filament using a number of relatively short high-power pulses and allowing rapid quenching to reform the highly resistive amorphous phase. However, there are a number of important differences between the a-Si and the chalcogenide memories: (a) it has been established that the a-Si memories do not form or WRITE at constant power; in general forming occurs at much lower powers ($<10^{-6}$) than in the chalcogenides ($10^{-4}$ - $10^{-3}$); (b) the forming, WRITE and ERASE operations for the a-Si memories are generally polarity dependent; (c) no rise in the temperature of the a-Si specimens can be observed immediately prior to switching; and (d) the a-Si WRITE and ERASE times are many orders of magnitude faster than those for the chalcogenides e.g. for the WRITE operation $10^{-8}$s compared with $10^{-3}$. For all these reasons we do not believe that the crystalline/amorphous thermal model is applicable to a-Si.

6.2.2. Models based on Trapped Space Charge

In many respects the behaviour of the amorphous Si layers appears to be closely related to that of crystalline Si MISS structures in that both show fast polarity dependent switching, both show current instabilities during some stage of the forming processes and both have high conductance states associated with current filaments. The major difference of course is that the MISS structures are threshold switches which always revert to the OFF-state when the power is
removed, whereas the a-Si layers have the additional advantage (and complexity) of non-volatile memory behaviour.

It is nonetheless possible that the memory switching in the a-Si devices is closely related to the mechanisms proposed for the MISS layers. Essentially two models have been used to explain the MISS behaviour\(^\text{13}\). These are generally referred to as "punch-through" and the "avalanche-mode" and both rely for switching on establishing high fields across space charge barriers in the films. In addition, in both models the low impedance state is produced by injected charge causing inversion of the Si at the Si/insulator interface. It is tempting to suggest that the "permanent" memory of the a-Si layers may be produced by a similar mechanism in which the charge is trapped in deep gap states at the insulator-semiconductor interface for which the probability of release is very small. However, the a-Si layers retain their memory without any observable change in their properties for as long as we have measured them, namely, for over one year at room temperature and 24 hours at 95°C.

Using the thermal release time from deep mid-gap states as a measure of the persistence of the trapped space charge, then from the well-known expression for the average thermal release time we estimate that the capture cross-section of these centres should be less than \(10^{-16}\) cm\(^2\). Although extremely small, such values would be consistent with Coulomb repulsive centres identified in crystalline materials\(^\text{14}\). However, the problem is that recombination of the trapped distribution through tunnelling or diffusion may well invalidate the above estimate by leading to a much faster decay of any trapped space charge distribution. All one can say at present is that a model in which the observed memory is associated with a trapped space charge cannot be excluded but, in view of the remarkable non-volatility of the memory states, may not be the correct explanation.

6.2.3. Other suggestions

It should be remembered that in the random network of the a-Si layers significant amounts of hydrogen are incorporated. The possibility therefore exists that memory switching may be associated with some atomic motion of hydrogen in the material. For instance, it has been reported that in ambient sensors containing Pd/a-Si Schottky barriers, hydrogen plays an important role in lowering the barrier\(^\text{15}\). Also the polarity dependence of the threshold voltages for the a-Si memories could be understood on the basis of field assisted hydrogen diffusion. Like all the possibilities mentioned above, this remains at present somewhat speculative and further work is required to identify the most likely memory switching mechanism.

7. CONCLUSIONS

A number of new results, including the observation of a filamentary ON-state,
Switching mechanism in amorphous silicon junctions

are reported in this paper. These provide important information relating to
the physical processes underlying the operation of the a-Si memories.

At present we believe that the initial stages of memory formation are likely
to be associated with high fields and/or trapped charges in a manner analogous
to that responsible for the threshold switching in crystalline Si MIISS devices.
However, neither the nature of the ON-state current filament nor the physical
mechanisms responsible for the permanent memory of the a-Si layers, have been
established with any certainty at the present time.

ACKNOWLEDGEMENTS

We should like to thank S. Kinmond and A. Carrie for their help with the
specimen preparation. The financial support of the B.P. Venture Research Unit
for some of the work described in this paper is gratefully acknowledged.

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A memory device comprising an electrically conducting substrate and layers of p, n and optionally i types of amorphous or microcrystalline semiconducting material, e.g. silicon, is formed by applying a forming voltage which is sufficiently large to cause the structure to be permanently modified to reduce the electrical resistance of the layers, this forming voltage being applied at elevated temperature preferably in the range 50°C to 300°C. Raising the temperature reduces the forming voltage.
This invention relates to a method for the forming of a non-volatile memory device incorporating amorphous or microcrystalline semiconducting material.


discloses an electrically programmable non-volatile semiconductor memory device. In its simplest form this contains p and n layers of amorphous silicon deposited onto a conducting stainless steel substrate. The layered structure is conditioned into a memory device by applying a large forward bias of known polarity which switches the structure into a stable ON state. This step is known as "forming" and permanently modifies the electrical properties of the device.

The forming voltage is approximately 20 to 25 volts. After forming the device can then be switched to the alternative OFF state by applying a voltage pulse above a low threshold such as 4-5V with opposite polarity to the original pulse. The OFF state is stable for voltage swings of ± 4-5V beyond which it switches to the ON state, i.e. the reverse threshold voltage \( V_{on} \) is ±4-5V. The ON state is stable for voltage swings of ± 1 volt beyond which it switches to the OFF state, i.e. the forward threshold voltage \( V_{on} \) is 4-5V. Switching times are remarkably fast, being less than 100 ns.

It is reported in this paper that \( V_{on} \) and \( V_{on} \) for the amorphous silicon devices investigated are at most only weakly temperature dependent.

We have now discovered that the applied voltage necessary for forming is a function of temperature, and that by increasing the temperature, the applied voltage can be reduced. Thus according to the present invention there is provided a method for forming a memory device comprising an electrically conducting substrate and layers of p, n and optionally \( i \) types of amorphous or microcrystalline semiconducting material, which method comprises applying to the substrate and layers a forming voltage sufficiently large to cause the structure to be permanently modified to reduce the electrical resistance of the layers wherein the voltage is applied at elevated temperature.

The elevated temperature should not be greater than 350°C. Preferably the voltage is applied at a temperature in the range 50 to 300°C.

We have further discovered that for any given forming temperature, there is a critical voltage \( V_{crit} \) above which and below which the required duration of the forming pulse is approximately independent of both voltage and temperature and that non-volatile memory devices formed at voltages above this critical voltage tend to have better properties than those formed at voltages below, particularly in respect of the ON-state resistance.

Most preferably layers of p-type and n-type amorphous or microcrystalline semiconducting material are deposited on the substrate to form a p-n configuration. Other combinations and sequences are also envisaged, however.

It is to be understood that p-type and n-type include \( p^+ \), \( p^- \), \( n^+ \), and \( n^- \) within their respective scopes.

The amorphous or microcrystalline semiconducting material is preferably amorphous silicon. Other semiconducting materials such as germanium are also suitable. The substrate can be stainless steel or a modified glass, the surface of which has been rendered electrically conducting by a layer of tin oxide, indium tin oxide or other light permeable electrical conducting material. An advantage of using an optically transparent substrate is that light may be used to affect the stable states of the device. The substrate may also be a similarly treated quartz.

Contacts for the device should include one or more electrically conducting areas on the outer surface of the layer remote from the substrate. These areas can conveniently be provided by strips or spots of a metal such as aluminium.

The layers of \( p \) type material can be prepared by methods known in the art, for example by decomposing a gaseous hydrogen-containing precursor of the material, e.g. silane, in a glow discharge. The layers of \( n \) type material can be prepared by adding diborane or phosphine respectively in varying quantities to the precursor.

The invention is illustrated by the following example and the accompanying Figure.

The results reported below were obtained on devices having a-Si doped and intrinsic layers in the sequence indicator. The a-Si was deposited by the glow discharge technique, with gas phase doping when appropriate. Stainless steel substrates were used.

A typical device possessed the following properties:
Log delay time ($T_D$) vs Applied voltage for the forming process.

**KEY:**
- $30^\circ$C.
- $80^\circ$C.
- $160^\circ$C.

**Diagram:**
- Log scale for $T_D$ (seconds)
- Voltage (VOLTS) axis
- Curves for different temperatures
- $V_{CR}$ threshold indicated
Continued.

The forming process, i.e. the first OFF-ON transition, does not occur instantaneously when a voltage step or pulse is applied to the a-Si p-n-i device. Initially there is a delay time, $t_0$, during which the device current remains essentially constant at the OFF-state value. The forming delay time is an extremely sensitive function of the applied voltage and typical data, obtained at three temperatures, are illustrated in the Figure. The forming delay time varies over nearly ten orders of magnitude from a few hundred seconds at low forming voltages to about 10 ns at high voltages. In particular, at a temperature dependent critical voltage $V_{cr}$, there is virtually a discontinuous change in $t_0$ as a function of bias. $V_{cr}$ corresponds approximately to the forming voltage which would be obtained in an experiment on a virgin device with a curve tracer. Note that above and below $V_{cr}$ the delay time tends to a value which seems to be approximately independent of both voltage and temperature; for the particular results illustrated $t_0$ is in the range $10^{-5}$ to $10^2$ s for $V<V_{cr}$ and in the range $10^{-10}$ to $100$ ns for $V>V_{cr}$.

CLAIMS

1. A method for forming a memory device comprising an electrically conducting substrate and layers of p, n and optionally i types of amorphous or microcrystalline, semiconductor material, which method comprises applying to the substrate and layers a forming voltage sufficiently large to cause the structure to be permanently modified to reduce the electrical resistance of the layers wherein the voltage is applied at elevated temperature.

2. A method according to claim 1 wherein the temperature does not exceed 350°C.

3. A method according to claim 2 wherein the temperature is in the range 50 to 300°C.

4. A method according to any of the preceding claims wherein the forming voltage is above the critical voltage as hereinbefore defined.

5. A method according to any of the preceding claims wherein the layers of p-type and n-type semiconductor material are deposited on to the substrate to form a p-n configuration.

6. A method according to any of the preceding claims wherein the semiconductor material is amorphous silicon.

7. A method as hereinbefore described with reference to the Example Memory devices whenever formed by a method according to any of the preceding claims.
The invention is a method of operating a semiconductor device having a layer of p-type amorphous or microcrystalline semiconductor in contact with an amorphous or microcrystalline semiconductor material of different conductivity type, and whose electrical properties have been modified by the application of a modifying voltage. The device exhibits threshold switching between lower and higher conductance states provided it is not switched to the maximum conductance or fully-on state. Switching between lower intermediate and higher intermediate states is envisaged.

![Current vs Voltage Graph]

**Threshold Switch**
SPECIFICATION

Threshold switch

5 This invention relates to threshold switching. Two types of switching are possible with semiconductor devices which can switch states of different conductivity. The device may start in one conductance state, switch to a second conductance state when the voltage applied to it exceeds a given threshold voltage and revert to the first conductance state when the voltage falls below the threshold value. Such behaviour is known as threshold switching.

In an alternative form of switching the device starts with a given conductance state and as the voltage applied to it is changed, switches to a second conductance state, which it retains when the voltage falls below the value which caused the initial change in conductance. The device is said to have "memory" of the second conductance state, even through the conditions initially responsible for it are no longer present, and the switch is described as a memory switch.

Integrated circuits described as "memories" are used in computers and similar apparatus. Such memories may be constructed from individual devices having either threshold or memory switching.

There have recently been disclosures of amorphous semiconductor devices showing memory switching based in layers of amorphous semiconductor material. Such memories may be constructed from individual devices having either threshold or memory switching.

We have now found that amorphous or microcrystalline junction semiconductor devices containing a p-layer and which have been subjected to a modifying voltage may be operated as threshold switches.

According to the present invention the method of operating a semiconductor device having an electrically conducting substrate and a layer of p-type amorphous or microcrystalline semiconductor material of different conductivity type and whose electrical properties have been modified by the application of a modifying voltage gives rise to the effect that the device in a lower conductance state switches to a higher conductance state when a voltage above a threshold voltage is applied to it, switching to a lower conductance state when the voltage is above a threshold voltage.

The disclosure by den Boor would not on the basis of the present invention the method of operating a semiconductor device having an electrically conducting substrate and a layer of p-type amorphous or microcrystalline semiconductor material of different conductivity type and whose electrical properties have been modified by the application of a modifying voltage gives rise to the effect that the device in a lower conductance state switches to a higher conductance state when a voltage above a threshold voltage is applied to it, switching to a lower conductance state when the voltage is above a threshold voltage.

The switching times available with amorphous semiconductor devices are of the order of 1 ms. For small over voltages above the threshold voltage the delay time before switching is at the order of 1 ms.

The disclosure by den Boor would not on the basis of the present invention the method of operating a semiconductor device having an electrically conducting substrate and a layer of p-type amorphous or microcrystalline semiconductor material of different conductivity type and whose electrical properties have been modified by the application of a modifying voltage gives rise to the effect that the device in a lower conductance state switches to a higher conductance state when a voltage above a threshold voltage is applied to it, switching to a lower conductance state when the voltage is above a threshold voltage.

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A device having a conductance state which is lower than the ON state of a similar device which has been formed into a memory device but above that of the OFF state is in an INTERMEDIATE conductance state.

The HIGHER conductance state of the present invention is an INTERMEDIATE state.

The modifying voltage applied to the device may be sufficiently high to "form" it into a memory device of the type described in the IEE Proc. paper or EP 95283 mentioned above. However the modifying voltage may be only sufficient to transform the device to an INTERMEDIATE conductance state.

The LOWER conductance state may be the OFF state or may be a LOWER INTERMEDIATE conductance state which is lower than the HIGHER state mentioned above.

Suitable forward bias switching voltages are in the range +2 to +10, preferably +3 to +6 volts. Such voltages are compatible with CMOS circuitry, unlike the threshold voltages of 10–35 V disclosed in App. Phys. Lett.

The speed of switching from LOWER to HIGHER conductance states and vice versa is less than 10 ns, compared with delay times of the order of 1 ms in the devices disclosed in App. Phys. Lett.

Suitable structures include layers having the configuration p-i-n, p-i-n, p-i and p-i-n. A further layer can be added to p-n type structures to give p-n-n or p-n-n type structures. The p, n or i-type amorphous or microcrystalline semiconductor material is a material which can be doped to provide p or n type conductivity (and in the case of p-and n-type material has been doped). For doping to be practicable the density of states in the gap between the valence band and the conduction band must be reduced to relatively low levels.

The existence of a high density of states has been attributed to the presence of "dangling bonds". Techniques for reducing the density of states in amorphous and microcrystalline semiconductor material e.g. silicon are well-known. Thus the semiconductor material may be deposited in the presence of hydrogen or may be treated with hydrogen after deposition.

Group IV of the Periodic Table, e.g. Si. Ge, and components thereof e.g. SiC.

The layers of semiconductor material may be such as to produce homojunctions in which there is a junction between layers of the same material thus having the same band gap e.g. silicon. The device may also be a heterojunction device i.e. there is a junction between different materials having different band gaps e.g. silicon and silicon carbide.

Desirably the device includes one or more electrically conducting areas on the surface of the silicon or indium tin oxide or other visible or ultra-violet light permeable electrically conducting material is a convenient substrate.

Alternatively the substrate can be similarly treated with doped or undoped layers on a support or metal sheets. Examples of metals are stainless steel and chromium.

The modifying voltages required to produce a device having an INTERMEDIATE conductivity state may be determined by simple tests on samples of the device. The invention is illustrated by the following Examples and the accompanying drawings.

**Example 1**

A semiconductor structure was prepared having a-Si doped and intrinsic layers in the sequence p+n-i. The a-Si was deposited by the glow discharge technique, with gas phase doping. A stainless steel substrate was used. The total thickness of the deposited layers was between 0.5 and 1.0 micron. After completion of the a-Si deposition, a series of NiCr dots was evaporated onto the silicon. The structure was modified into a device by applying a bias voltage to the dot.
forward bias of 25 V, the p region being positively biased. The application of the modifying voltage produced the INTERMEDIATE state directly. Its resistance in this state was 3 kilo-ohm measured at 0.1 V.

The device was then tested by applying increasing forward bias voltages and measuring the current passed. The current-voltage characteristics are plotted in Curve A of the accompanying drawing. As the voltage was increased a point was reached (3V) at which the current suddenly switched to a higher range, representing a change to a higher INTERMEDIATE conductance state. A subsequent reduction in voltage caused a reversion to the original INTERMEDIATE state at a somewhat lower voltage (2.8 V) because of hysteresis.

The device was thus initially modified into the LOWER state (in this case a lower INTERMEDIATE state) and was then switched to the HIGHER (in this case a higher INTERMEDIATE state) by a small forward bias. The device could be switched between the two INTERMEDIATE conductance states (HIGHER and LOWER) by applying voltages above and below the threshold voltage.

Example 2

Example 1 was repeated with a similar device having a glass substrate and a resistance in the INTERMEDIATE state into which it was first modified of 25 kilo-ohm at 0.1 V. Current-voltage characteristics are plotted in Curve B. A similar effect to that of Example 1 was noted at a threshold voltage of about 6 V. Thus the device was again first modified into a LOWER (INTERMEDIATE) state and then subsequently switched between this LOWER state and a HIGHER (INTERMEDIATE) state of higher conductance.

CLAIMS

1. A method of operating a semiconductor device having an electrically conducting substrate and a layer of p-type amorphous or semiconductor in contact with an amorphous or microcrystalline semiconductor material of different conductivity type and whose electrical properties have been modified by the application of a modifying voltage is characterised by applying to the device in a LOWER conductance state a voltage above a threshold voltage sufficient to switch the device to an HIGHER conductance state and thereafter successively applying voltages below and above the threshold voltage to switch between the HIGHER and LOWER states.

2. A method according to claim 1 wherein the device has been modified by application of a voltage sufficient to transform the device to an INTERMEDIATE conductance state.

3. A method according to either of claims 1 or 2 wherein the device is switched be-