UNIVERSITY OF EDINBURGH THESIS

Author (surname, initials): Breslin, J. A.  
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Novel Pixel Circuits
for Liquid Crystal over Silicon
Spatial Light Modulators

John A. Breslin

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Abstract

Spatial Light Modulators are used in many applications and Liquid Crystal Spatial Light Modulators are a mature technology with devices now commercially available. Over the past 3 years there has been a rapid increase in device resolution, with a decrease in pixel size. To date though, on Static Memory pixels that incorporate charge-balancing circuitry, the underlying pixel architecture has remained unchanged.

This thesis presents novel “load-and-display” Static Memory pixel designs. The importance of the pixels’ architectural changes is highlighted, along with design and implementation issues.

The thesis also presents two more specialised pixel architectures: pixels designed for a specific application, rather than as general purpose load-and-display devices.

Future trends in Liquid Crystal Spatial Light Modulators are also considered: has research and development now reached steady-state; or what impact could the designs presented in this thesis in conjunction with changes in silicon process technology have on these future trends?
Declaration

I declare that this thesis has been completed by myself and that, except where indicated to the contrary, the research documented is entirely my own.

John A. Breslin
Acknowledgements

Over the course of my PhD studies I have met a large number of great people — many of whom have given up some of their valuable time to help me. These acknowledgements don’t really do them justice, but I’ll give it a try.

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It’s been brilliant, absolutely brilliant, I’ve met a bunch of really wonderful people — including Catherine, my wife \(^1\) — made some great friends, and had a stonking time.

Cheers!

\(^1\)But that’s another story.
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To Mum and Dad,

and Catherine.
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The Coming of the Wee Malkies

by Stephen Mulrine

Whit'll ye dae when the wee malkies come,
if they dreep doon affy the wash-hoose dyke,
an pit the hems oan the sterrheid light,
an play wee heidies oan the clean close-wa,
an blooter yir windae in wi the baw,
missis, whit'll ye dae?

Whit'll ye dae when the wee malkies come,
if they chap yir door an choke the drain,
an caw the feet frae yir sapsy wean,
an tummle thur wulkies through yir sheets,
an tim thur ashes oot in the street,
missis, whit'll ye dae?

Whit'll ye dae when the wee malkies come,
if they chuck their screwtaps doon the pan,
an stick the heid oan the sanit'ry man;
when ye hear thum shauchlin doon yir loaby,
chantin, “Wee Malkies! The gemme’s a bogey!”
— Haw, missis, whit’ll ye dae?
Chapter 1

Introduction

1.1 Background

Spatial Light Modulators (SLMs) are used in many optical systems from simple displays to complex optical correlators. The SLM devices can be implemented in a variety of technologies, including Multiple Quantum Well (MQW) structures; Deformable or digital switchable Mirror Devices (DMDs); and Liquid Crystals (LCs) as modulating materials.

Liquid Crystal SLMs are a mature technology, offering a high pixel count, inexpensive and straightforward manufacture, and good optical quality. Pixel circuits for these devices can be based on Dynamic or Static Random Access Memory (RAM) circuits — there are advantages and disadvantages for both.

This thesis presents work carried out in the development of new Static RAM pixel circuits for implementation in “load-and-display” pixels, and also for more specialised devices.

The thesis also discusses future trends in Silicon Process Technology and what impact these developments may have on Liquid Crystal over Silicon Spatial Light Modulators.
1.2 Thesis Outline

- Chapter 2 reviews selected SLM technologies. A selection of modulating techniques is described with some modes of operation, advantages, disadvantages, etcetera. Liquid Crystal materials and devices are described in more detail.

- Chapter 3 describes liquid crystal spatial light modulators and the pixel circuits used in these devices. Static and Dynamic RAM pixels are discussed with their advantages and disadvantages. Chapter 3 also discusses future trends in silicon CMOS processing and their potential impact on future Liquid Crystal over Silicon SLM devices.

- Chapter 4 presents the new pixel circuits for load-and-display Static RAM pixels with charge-balancing circuitry. The advantages of these circuits are discussed, comparisons are made with existing pixels, and design issues are highlighted.

- Chapter 5 discusses the implementation of the novel pixel circuits on real silicon devices. Implementation issues and techniques for tackling them are presented.

- Chapter 6 presents optical and electrical results taken from the silicon devices discussed in Chapter 5. Measurement techniques are explained as are difficulties encountered when testing the devices.

- Chapter 7 describes two novel smart pixel circuits. These smart pixels are specialised devices design for specific applications. The motivation behind their conception is presented along with design issues and preliminary results from implementation on silicon.

- Chapter 8 summarises the work presented in this thesis and discusses what conclusions can be drawn. In addition, some suggestions are made for
further work that could be carried out on aspects of research presented in this thesis.

• Appendix A contains the author’s publications.

• Appendix B contains a mathematical proof that was derived to calculate the resistance of a polygon conducting segment.

• Appendix C presents research that was carried out in the modelling of current behaviour in conducting wires. Mathematical proofs are presented along with simulation results.

• Appendix D contains some of the reference material that the author has used whilst carrying out research and writing this thesis.
Chapter 2

A Review of Selected Spatial Light Modulator Technologies

In this chapter I summarise several SLM technologies. Liquid crystal methods are considered in more detail, as it is this technology that is used with the pixel devices presented in this thesis.

2.1 Introduction

Spatial Light Modulators are devices that are capable of modulating one or more properties (for example amplitude, phase, polarisation, etcetera), of an incident optical wavefront (i.e. a beam of light). The devices vary in their complexity and modes of operation. For example, a concave mirror, or a pair of sunglasses could be considered crude forms of SLM.

SLMs are used in a wide variety of applications, for example,

- Displays and projection systems [1] [2] [3] [4] [5].

- Optical Correlators [6].

- Wavefront Aberration Correction Systems [7].
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

- Neural Networks [12] [13].
- Other Optical Systems [14].

An SLM consists of an nxm array of pixels each of which can be switched into one of two optical states (in the case of binary devices), or can be switched into one of a number of states if some analogue mode of operation is used (see Figure 2–1).

![Figure 2–1: A reflective Spatial Light Modulator Pixel Array. The optical state of a pixel is represented by the density of shading.](image)

The devices themselves can be addressed in different ways and can have many different pixel implementations.

### 2.2 Pixel/SLM Implementations and Classifications

Pixels can be implemented in many different ways. Some pixel designs will be highly dependent on the way the SLM itself is implemented. However at a higher level of abstraction, pixels can be grouped into two categories.
2.2.1 Load-and-Display Pixels

Load-and-Display pixels are devices that are loaded with some value that can be analogue or digital and "display" this value (see Figure 2–2).

![Diagram of a Load-and-Display Pixel](image)

**Figure 2–2**: A Load-and-Display Pixel. The DATA and LOAD signals can be common to a row and column so that arrays of pixels can be loaded one line at a time.

2.2.2 Smart Pixels

A Smart Pixel is a device that can have one or more optical inputs and one or more optical outputs, with electrical connections — control signals and possibly local connectivity — between pixels.

On-pixel circuitry can perform complex, smart operations on data input: addition, multiplication, comparison, and route results back into the optical domain [15] [16] (see Figure 2–3).

\[1\]The word “display” may be slightly misleading as this value may not affect the intensity of the modulated light, but may for example, modulate phase or polarisation.
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

Figure 2-3: A Smart Pixel Array. The array shows incident and modulated or emitted light waves, and local connectivity between pixels.

2.2.3 Electrically and Optically Addressed Pixels and SLMs

The way that data and/or control signals are loaded onto an SLM defines whether it is classed as an Electrically Addressed SLM (EASLM), or Optically Addressed SLM (OASLM) — or both.

EASLMs

An EASLM is a device in which data and/or control signals are loaded electrically. That is, the “values” or “states” the pixels have (for example ON or OFF), are
loaded in electrically via some interface board and/or some host computer (see Figure 2-4).

![Electrically Addressed SLM Pixels](image)

**Figure 2-4**: Electrically Addressed SLM Pixels. The example shown is of amplitude modulation. The “on” pixel reflects incident light, the “off” pixel absorbs it.

**OASLMs**

An OASLM is a device in which data signals are loaded optically i.e. the light modulating properties of a pixel can be controlled using an optical signal [17]. These devices may still have some electrical connectivity (for example a power supply).

![Optically Addressed SLM Pixels](image)

**Figure 2-5**: Optically Addressed SLM Pixels. The example shown is of amplitude modulation. The “on” pixel reflects incident light, the “off” pixel absorbs it.
2.2.4 Transmissive and Reflective Devices

A transmissive device is one where the incoming (modulated) light beam is transmitted through the modulating cell.

A reflective device is one where the incoming light beam is reflected back from the modulating cell (see Figure 2–6).

![Figure 2-6: Transmissive and Reflective SLM Pixels.](image)

2.3 SLM Technologies

The following sections summarise several SLM technologies. The technologies considered are mature, have immediate commercial applications, and use different techniques to effect light modulation.

2.3.1 Self Electro-optic Effect Devices

Self Electro-optic Effect Devices (SEEDs), are implemented using a PIN diode where the 'I' (Intrinsic), region is formed from a Multiple Quantum Well (MQW)
material. SEEDs can operate as optical receivers and modulators, and there are several implementation methods for such devices.

For further information on S-SEED devices, the reader is referred to [18] [19] [20].

S-SEED Receivers

Symmetrical-SEED receivers use two reverse-biased PIN diodes to produce an electrical signal (see 2–7):

![Diagram of S-SEED Receiver](image)

**Figure 2–7:** An S-SEED Receiver. Light can be shone in sequence on the two diodes allowing charge to be deposited on or removed from the output node. Circuitry can be connected to the output node to generate a digital signal from the output charge.

When light is shone on the bottom diode, photo-current causes electrons to accumulate at the common **OUTPUT** node and produce a voltage. This voltage will be given by:

\[
V = \frac{Q}{C}
\] (2.1)
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

Where $Q$ is the amount of charge deposited, and $C$ the capacitance seen from the node. When light is shone on the top diode a positive charge is deposited at the common node and the output voltage is changed.

S-SEED Modulators

To operate the device as a modulator, an input voltage and an incident light beam must be supplied to the S-SEED. If the input voltage swing is high enough, the reflectivity of the device will be high and the incident light will be reflected. This is because the electron from the electron-hole pair created by the incident light will be forced to recombine with its hole partner. If the voltage swing is low, the reflectivity will be low, and the device will remain dark — as the electron will move to the conduction band causing complete absorption of the photon (see Figure 2-8):

![Diagram of S-SEED Modulator](#)

**Figure 2-8:** An S-SEED Modulator. The output node ($V_{in}$), may require to be interfaced to specially designed driver circuitry for the S-SEED.

Note that in both cases two optical signals are required as two PIN diodes are being used.

The major advantage of S-SEED devices is their high switching speeds (several pico-seconds) [21], and thus they have uses in high-speed non-display applications such as telecommunication switching.
However they have several disadvantages: they can be optically bandwidth limited, with devices operating in the 840→860nm or the 1047→1064nm wavebands [22] [23], thus S-SEEDs are not suited for displays. They can have a poor contrast ratio \(^2\) (3:1) [25]. The wafers on which the SEED diodes are manufactured are not suited to monolithic integration of other circuitry. Other functionality — such as the the driving circuits — is usually implemented on a silicon CMOS chip onto which the SEED array is flip-chip bonded (glued). S-SEEDs may also require high biasing voltages (+10V) [21], and the S-SEEDs — with the CMOS driving circuitry — may have large current requirements and power consumption (for example, 1.1mA of static current drawn on a SEED receiver on a 0.8\(\mu\)m CMOS process [26]), and large area (6160\(\mu\)m\(^2\) for receiver circuitry and 1880\(\mu\)m\(^2\) for modulating circuitry on a 0.8\(\mu\)m process [26]). Therefore they may not be suited to large arrays.

2.3.2 Deformable and Digital Mirror Devices

Deformable Mirror Devices

Deformable Mirrors can consist of some form of membrane that is placed over a pixel array leaving a gap between the two. The membrane can be deformed by an electrostatic force by putting charge on the underlying pixels. This will phase shift or deflect light being reflected from the mirror (see Figure 2–9).

\(^2\)The Contrast Ratio \(C_r\) of a device can be defined as the ratio of the device’s maximum to minimum light throughput [24]
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

Figure 2-9: A Deformable Mirror. The diagram demonstrates a continuous membrane device overlaying a pixel array. Values stored at each pixel cause the membrane to be moved.

These devices have applications as phase modulators for wavefront correction systems [7]. They have a large optical bandwidth — as they are mirrors — and a very high contrast ratio. However, they can have a low switching speed (2ms), and may require large voltages to deform the membrane (+30V → +250V).

Digital Micromirror Devices

Digital micromirror devices consist of an array of pixels, where each pixel is formed from a mirror that is hinged over addressing circuitry on an underlying silicon substrate (see Figure 2-10) [27].

Figure 2-10: A Digital Mirror Pixel. The mirror device can be placed over a memory cell (for example an SRAM circuit). The value stored in the cell can cause the mirror to switch on its hinge.

The addressing circuitry can be some form of SRAM array so that mirrors are flipped between one of two binary states (ON or OFF) (see Figure 2-11).
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

2.3.3 Liquid Crystal Devices

Liquid Crystal SLMs can be implemented in a variety of ways using a variety of liquid crystal materials, and can be used to modulate light amplitude, phase, and polarisation.

LC devices can be implemented as being transmissive, where the light wave passes between two transmissive plates or as reflective. In this latter case, the SLM is constructed by gluing a cover glass onto a backplane which contains the pixels. In the case of liquid crystal over silicon devices, this backplane is a silicon die. The inside of the cover glass is coated with a transparent conductor (for example indium tin oxide), and a gap is maintained between the glass and the silicon by using spacer materials in the glue or on the pixel array (see Figure 2-12).

Figure 2-11: Digital Mirror Pixel Operation. The value stored in the underlying memory cell causes the mirror to deflect or not.

These devices have a high contrast ratio, and a fast switching speed (20μs) [28]. Also — as they are mirrors — they have a wide optical bandwidth.

These devices are produced by Texas Instruments, and their main application is in display and projection systems [3].
Figure 2-12: A Reflective Liquid Crystal SLM. The diagram shows the cross-section of such a device (not to scale). Liquid crystal alignment layers — if required — can be manufactured on the ITO electrode and the pixels.

These devices are referred to as Liquid Crystal over Silicon Spatial Light Modulators (LCOS SLMs).

It is desirable in these devices to maintain a uniform cell thickness across the array, and to maintain array flatness. This is to achieve a high optical quality (see Equation 2.4).

Liquid Crystal Materials

Liquid Crystals are materials that exist in a phase between the liquid state and the crystal state state. LC materials generally consist of long thin molecules which are formed by joining aromatic rings to hydrocarbon chains [29] [30] [31] [32] (see Figure 2-13).
Liquid Crystals can exist in a variety of meso-phases [33] which are dependent on temperature (see Figure 2-14).
Liquid crystal materials are birefringent. This means that the materials can possess an ordinary and an extraordinary optical axis.

Light passing along the ordinary axis will travel at a different speed to that of light passing along the extraordinary axis — this introduces a phase difference between the two light rays and can also alter the polarisation state(s) of the light as it travels through the material.

For further information the reader is referred to [34].

When a liquid crystal material is sandwiched between two electrodes, an electric field applied between the two electrodes can cause the material's molecular
orientation and/or position of polarisation vector and/or optical axes to change (see Figure 2-15), this changes the optical properties of the LC \cite{35} \cite{36}.

\begin{center}
\begin{tikzpicture}

\node[draw=black,thick,align=center] (a) at (0,0) {LC Material};
\node[draw=black,thick,align=center] (b) at (2,0) {Electrodes};
\node[draw=black,thick,align=center] (c) at (0,-1) {No Voltage};
\node[draw=black,thick,align=center] (d) at (2,-1) {Applied Voltage};

\draw[<->,thick] (a) -- (b);
\draw[<->,thick] (c) -- (d);
\end{tikzpicture}
\end{center}

\textbf{Figure 2-15:} Liquid Crystal Switching. As the voltage across the LC material is altered, the molecular orientation of the material can be changed.

These properties of Liquid Crystal materials can be used to modulate the phase and amplitude of light rays (in the infra-red as well as the visible optical wavebands).

\textbf{Charge Balancing} A requirement of LC materials is that they be \textit{charge-balanced}. This means that a voltage of \(+V\) applied for \(t\) seconds, must be followed by a voltage of \(-V\) for \(t\) seconds \(^3\); otherwise the LC material degrades due to electrochemical decomposition \cite{37}\cite{38}. That is, the time-averaged (net d.c.) voltage across the LC must be zero.

\textbf{Ferroelectric Liquid Crystals} Ferroelectric liquid crystals can have a structure similar to the Smectic C phase seen in Figure 2-14, except that the molecules have a helical progression between layers \cite{39}. That is, the molecules are rotated slightly on progressing layers. This phase is labelled SmC* \cite{40} (see Figure 2-16).

\(^3\)Alternatively, a pulse of \(-V/2\) could be applied for \(2t\) seconds — the material will charge-balance as long as the voltage magnitude \(x\) time constant is equal.
Ferroelectric materials can have a high switching speed (200ns) [41], and can be used to modulate the amplitude and phase of light.

The ferroelectric liquid crystal molecules exhibit a \textit{Spontaneous Polarisation Vector} $P_S$, that points at right angles to the LC molecule. In the normal helical progression the average value of this vector is zero. However by suppressing the helical progression — by forcing the molecules to lie "flat" — the average value of $P_S$ can be made non-zero.

The helical progression is suppressed by having a narrow gap between the cell electrodes, and by using parallel alignment layers in which the molecules can lie (see Figure 2–17), and align to [42] [43].
Figure 2–17: Liquid Crystal Alignment Layers. Liquid crystal molecules can lie inside the alignment layers. Molecules in successive vertical layers will align in the same direction.

These alignment layers can be polished or grown onto the appropriate surface by deposition of silicon dioxide.

This configuration is known as Surface-Stabilised Ferroelectric Liquid Crystal (SSFLC) [44] (see Figure 2–18).
Figure 2–18: Switching of a Bistable SSFLC Molecule. Applying the appropriate charge determined by \( Q = 2|P_S|A \), will cause the FLC molecule to switch between states.

The suppression of the helical progression causes the SSFLC to exhibit bistability and hysteresis. That is, the FLC molecules and polarisation vectors can only switch between two stable states \(^4\) unlike nematic LCs, and some other forms of FLC which exhibit analogue switching.

Hysteresis means that once switched to the "ON" state, the FLC will remain in this state until it receives an equal and opposite amount of charge, then it will switch to the "OFF" state.

For example, in CMOS applications, a +5V pulse applied to an FLC pixel will turn the pixel ON. The pixel will (ideally), remain ON when the pulse is

\(^4\)Ideally that is. However, due to poor alignment and/or defects in the liquid crystal, full bistability and hysteresis is often not achieved — the SSFLC may for example, exhibit limited analogue switching.
removed (i.e. when the voltage drops to 0V). The pixel will only turn OFF when a pulse of $-5V$ is applied (this will be discussed later).

The $P_s$ value of an SSFLC is measured in charge per unit area (usually $nC/cm^2$), for example: $50nC/cm^2$; and the charge on the bounding plates required to switch the FLC fully from one state to another is given by:

$$Q = 2|P_s|A$$

(2.2)

Where $A$ is the area of the FLC material under the plates.

The switching time of the FLC is dependent on the $P_s$ value, the viscosity of the material ($\eta$), and the electric field ($E$) — the voltage — driving the material as follows:

$$t_s = \frac{\eta}{P_s E}$$

(2.3)

Thus, for high switching speeds, a low viscosity material, with a high spontaneous polarisation, and a high driving voltage, is desired.

The intensity of light passing through the FLC material is defined as follows:

$$I_{OUT} = I_{IN} \sin^2(2\phi) \sin^2\left(\frac{\Delta n d \pi}{\lambda}\right)$$

(2.4)

Where $I_{OUT}$ is the output intensity, $I_{IN}$ is the input intensity, $\phi$ is the alignment angle between the FLC and the polariser, $\Delta n$ is birefringence of the FLC, $d$ is the cell thickness (for a reflective LCOS device, the thickness will be $2d$), and $\lambda$ is the wavelength of the incident light.

Ferroelectric liquid crystals can offer fast switching (200ns) [41], high contrast ratios (>100:1) and are suited to applications that require fast optical switching and high optical efficiency.
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

Amplitude Modulation using SSFLC on an LCOS SLM  To effect amplitude modulation, polarised light is presented to the pixel array. A voltage applied across the liquid crystal rotates the polarisation of the light as it passes through the material. The “altered” light can be viewed through Polariser B, the unaltered light cannot, and so the pixel appears dark (see Figure 2–19).

![Figure 2–19: Amplitude Modulation using SSFLC on an LCOS SLM.](image)

Binary Phase Modulation using SSFLC on an LCOS SLM  Binary phase modulation can be effected by two methods.

The first method aligns the FLC material such that one of its optical axes is tangential to the input light ray. In one state (e.g. pixel OFF), the ordinary optical axis is tangential to the ray and the extraordinary optical axis lies along the path of the polarised input light ray. In the other state (e.g. pixel ON), the opposite happens (see Figure 2–20). The light will move at a different speed depending on what axis it travels along, therefore a different path length is travelled along each axis, and a phase difference is produced.
The second method has the input light ray bisect the ordinary and extra ordinary optical axes. As the light ray passes through the FLC material it becomes elliptically polarised i.e. extra polarisation "modes" are introduced. Switching the FLC causes a rotation of 45° in the axis and the direction of the elliptical polarisation is altered (i.e. the relative phase of the wave changes — see Figure 2–21). Polariser B is at 90° to A and so filters out the vertically polarised light leaving the horizontal beams that are π out-of-phase with one-another as desired.
Chapter 2. A Review of Selected Spatial Light Modulator Technologies

Polarizer A

FLC

Polarizer B

Figure 2-21: Binary Phase Modulation using SSFLC on an LCOS SLM: Method2.

Note, for simplicity, Figure 2-21 shows the light ray passing through a transmissive cell. This technique of phase modulation can be used on LCOS SLMs if required.

Other Ferroelectric Materials Other ferroelectric liquid crystal types exist which can be used to effect analogue modulation: using the electroclinic effect [45] [46], the distorted helix effect [47], or using antiferroelectric liquid crystals [41] [48, p.24].

These modes can have high switching speeds, but may require complex drive electronics and/or precise operating temperatures and/or addressing to maintain accurate analogue switching levels [41].

Liquid Crystal devices have applications in displays, optical correlators, and holographic switching applications that do not require high-data rates — they are capable of easily generating multi-phase holograms (unlike S-SEED devices [49] ), and this will be discussed in Chapter 7.
2.4 Summary

This chapter has discussed a number of modulating technologies and their operating principles. These are summarised below:

<table>
<thead>
<tr>
<th>Technology</th>
<th>Optical Bandwidth</th>
<th>Switching Speed</th>
<th>Contrast Ratio</th>
<th>Driving Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-SEED</td>
<td>very small infra-red</td>
<td>pico-seconds</td>
<td>3:1</td>
<td>+10V</td>
</tr>
<tr>
<td>Def. Mirror</td>
<td>$\infty$</td>
<td>$\approx$ 2ms</td>
<td>$\infty$</td>
<td>+30V</td>
</tr>
<tr>
<td>Digi. Mirror</td>
<td>$\infty$</td>
<td>20$\mu$s</td>
<td>$\infty$</td>
<td>+5V</td>
</tr>
<tr>
<td>Liquid Crystal</td>
<td>broad</td>
<td>200ns</td>
<td>$&gt;100:1$</td>
<td>$&lt;+5V$</td>
</tr>
</tbody>
</table>

*Table 2-1: A Summary of SLM Technologies.*

Liquid Crystal devices will be discussed in more detail in the next chapter.
Chapter 3

Liquid Crystal over Silicon Spatial Light Modulators

This chapter discusses Liquid Crystal over Silicon Spatial Light Modulators and the circuits used for load-and-display pixels. It also discusses what the expectations of the semiconductor industry are (up until the year 2010), in terms of (shrinking) process geometry, die area, supply voltage, and other related metrics; and what implications these could have for liquid crystal over silicon SLMs.
3.1 Introduction

As discussed in Chapter 2, Liquid Crystal over Silicon SLMs consist of an array of pixels manufactured on a silicon backplane with a coverglass placed over the pixel array and an LC material sandwiched between the two.

Load-and-display pixels store some electronic data value (a binary '1' or '0', or some analogue value), and normally contain some data and addressing lines which can be common to a row or column (see Figure 3–1).

![Figure 3–1: A generic load-and-display Liquid Crystal over Silicon SLM Pixel schematic.](image)

The ADDRESS ENABLE line is used to load the memory cell with new data that is present on the DATA line. This data value is used to drive the pixel mirror (i.e. the pixel) to its desired state — the pixel mirror being the area driving the liquid crystal in this case.

The pixel memory cell can be implemented using standard DRAM or SRAM memory cells. The pixel circuit in practice can depend on the requirements of the SLM.
3.2 Charge Balancing

Charge balancing — normally a requirement of liquid crystal SLMs — can be carried out by holding the front electrode at $V_{DD}/2$ and loading each pixel with a value and then its complement. Alternatively, the front electrode and the values in the pixel circuits can be toggled with some clock signal. This will be discussed more fully in later sections.

3.3 Planarisation

Planarisation is a procedure that can be used on liquid crystal over silicon SLMs to improve their optical quality and increase the Fill Factor.

The Fill Factor is a percentage given by: $\frac{\text{Mirror Area}}{\text{Pixel Area}} \times 100\%$ [50] (see Figure 3–2), and provides a measure of how much of the total pixel area is covered by the pixel mirror.

An SLM backplane pixel has two components: the pixel circuitry (formed from transistors), and the pixel mirror (formed from a square of metal).

In early devices, the pixel circuitry — DRAM or SRAM — took up some fraction of the pixel area and so reduced the Fill Factor. However, planarisation techniques have been devised to improve this fill factor.
When the silicon SLM wafers are received back from fabrication, postprocessing steps may be carried out to add layers of metal that cover the whole pixel. This increases the mirror area and the pixel fill factor (see Figures 3–3, 3–4). New techniques can give fill factors of almost 100% [51], and in some newer pixel layouts there is no pixel mirror seen in the pre-planarisation layout — just a connection to the planarisation layer [52] [53].
Chapter 3. Liquid Crystal over Silicon Spatial Light Modulators

Figure 3-3: A Planarised Pixel. a.) shows the top view of the pixel. b.) shows the pixel’s cross-section.

The additional layers of metal can be “polished” to improve the optical quality of the pixels.

Figure 3-4: Unplanarised and Planarised Pixels. a.) shows an SEM micrograph of an unplanarised pixel. b.) shows an SEM micrograph of a planarised pixel.
3.4 DRAM Pixels

DRAM pixels can be constructed from 1, 2, 3, and 4 transistors [54], [55], [56, pp.27-29] [57].

The 1 and 2 transistor pixels are similar in structure to standard 1 transistor DRAM memory cells (see Figure 3-5).

![Figure 3-5: 1 and 2 Transistor DRAM Pixels. a.) shows a 1T DRAM pixel where the pixel capacitance is formed from parasitics in the circuit. b.) shows a 2T DRAM pixel where the pixel capacitance is formed using a common source-drain transistor.]

A data value is written to the cell by enabling the WRITE line. The value is stored in the pixel capacitor. This capacitor is formed from parasitics between the pass transistor drain and the pixel mirror pad, and/or the substrate and the pixel mirror pad (depending on what level of capacitance is desired, and what the process parameters are).

In the case of the 2 transistor pixel, the capacitance is formed using the gate capacitance of a transistor with a common source and drain, as — for some processes — this will give a high value of capacitance per unit area and help to reduce charge leakage.

In both cases it is feasible to use PMOS instead of the NMOS transistors shown if desirable.
For such DRAM pixels in SSFLC devices it is desirable to make this capacitance large, as a charge of:

\[ C = \frac{2P_SA}{\Delta V} \]  

is required to switch the FLC. Where \( C \) is the pixel capacitance, \( P_S \) is the FLC spontaneous polarisation value, \( A \) is the area of the FLC addressed by the pixel (i.e. the pixel mirror area), and \( \Delta V \) is the voltage drop across the FLC (the equation is derived by substituting: \( CV = Q \) in Equation 2.2).

This means that the pixel capacitor can be quickly loaded with this charge and the next pixel row addressed. The alternative would be to address the pixel until the liquid crystal has switched and this switching time may be longer than the electrical addressing time.

Single transistor pixel circuits have several advantages and disadvantages in comparison with SRAM based designs:

- **DRAM Advantages.**
  - The circuits have low area.
  - The circuits have simple connectivity and few components.
  - They can store analogue or binary values.

- **DRAM Disadvantages.**
  - DRAM cells suffer from charge leakage (which can be increased by light falling on the cell), and must be refreshed.
  - Cells may only store a finite amount of charge.
  - DRAM SLMs can be complicated to charge balance. They may require an image then an inverse image to be loaded in order to maintain a net 0V d.c. voltage. This may mean that a pulsed light
source has to be used to view the SLM (the light is turned off when the inverse image is displayed). Some DRAM SLMs use blanking frames to turn the whole array on and off between image and inverse-image displays [54].

- DRAM SLMs can have a low Frame Rate.¹

This is because of the inverse image requirement (perhaps with blanking frames), that means at least a full (inverse) image must be loaded for every valid one.

- The inverse-image requirement (perhaps with blanking frames), complicates the addressing interface circuitry.

In spite of these disadvantages, DRAM pixels have been used in many large-array SLMs [58] because they have a low area.

¹ The Frame Rate is the number of valid frames a device can display per second.
3.5 SRAM Pixels

SRAM Pixels are based around standard 6 transistor SRAM memory cells [59] (see Figure 3-6),

![SRAM Cell Diagram](image)

**Figure 3-6**: A 6 Transistor SRAM Cell.

The feedback inverters hold the SRAM cell in a steady state (i.e. LATCH is HI, LATCHBAR is LO, or vice versa). To alter the contents of the cell, the ENABLE line is asserted \(^2\) and the new values are loaded on the D and DBAR lines. Since these data lines are trying to drive the SRAM cell into a new state, careful ratioing of the access transistor sizes and the circuitry driving the data lines at source, with respect to the inverters’ transistors may be required in order to have the cell reliably flip state [59] [60].

Some SRAM pixel implementations use a 6 transistor SRAM cell with an inverter buffer to drive the pixel mirror [57] (see Figure 3-7).

\(^2\)Note, the access transistors can be PMOS instead of NMOS if desired.
Figure 3-7: A simple SRAM Pixel. The pixel uses a 6 Transistor SRAM cell for data storage and an additional inverter buffer is used to drive the pixel mirror.

An SLM using such pixels still requires an inverse frame to be loaded in order to charge-balance the LC.

However, some implementations incorporate specialised circuitry to simplify charge-balancing. This circuitry currently takes the form of an XOR (or an XNOR) gate that is connected to the SRAM output (see Figure 3-8).
Charge balancing can be effected two ways. A global **CLOCK** signal is XORed with the stored data value (**LATCH**). This **CLOCK** signal is also present on the global front electrode (FE). If the pixel is storing a '1', the mirror experiences a $+V_{DD}$, $-V_{DD}$, transition over one clock period. This will turn the pixel ON, and then implement the charge balance (the mirror having a 50% duty cycle). If the pixel is storing a '0', the XOR output is in phase with **CLOCK**, so the mirror will have a zero voltage drop and remain off. In each case, the net d.c. voltage across the mirror is zero (see Figure 3-9) [61].
Figure 3-9: Charge Balancing Waveforms. This diagram shows typical charge balancing waveforms associated with the XOR-SRAM pixel.

This addressing scheme provides hard driving voltages for the liquid crystal as voltages of $\pm V_{DD}$ are used for the two drive states. It also means that no pulsed light source is required as an inverse-image is not displayed.

Alternatively the front electrode can be held at $V_{DD}/2$ as normal. This provides half the voltage swing of the former scheme and requires a pulsed light source to be used since the clock signal will display an image-inverse.

Whatever scheme is used, the extra circuitry means that charge balancing takes place over one clock cycle. Pixels without this circuitry require the whole SLM to be loaded with an inverse image which reduces the frame rate.

SRAM pixels demonstrate significant improvements in performance over DRAM devices but do have disadvantages

- SRAM Advantages.
The stored signal is electrically robust: they do not suffer from charge leakage.

They can provide better driving voltages for the pixel mirror and an unlimited supply of charge (i.e. $V_{DD}$ and $V_{SS}$), via the SRAM cell.

They can be viewed under a continuous light source because specialised charge balancing circuitry can be incorporated directly onto the SRAM cell.

A frame inverse-frame load with possible blanking frames is not required (unlike DRAM devices [54]).

SRAM devices can have a higher frame rate as charge balancing can be effected over one clock cycle.

• SRAM Disadvantages.

SRAM cells have a higher area than DRAM.

On identical processes, DRAM cells have been implemented with one quarter the area required by SRAM cells (see Table 3-1).

XOR SRAM cells can have a complex connectivity.

As many transistors (10) are being used in the pixel circuit, the connectivity of the circuit can be complex, unlike DRAM devices where only one transistor may be needed.

SRAM cells and SLMs can have a higher power consumption and larger current spikes than DRAM devices. This is explained below.

As the SRAM cell contains several components that can dissipate power when switching (i.e. the inverters and XOR circuitry) [62], transient current spikes and power consumption must be accounted for. DRAM cells having no such complex circuitry do not have the same current and power overheads.
Chapter 3. *Liquid Crystal over Silicon Spatial Light Modulators*

Clearly, if improvements to charge-balancing SRAM cells can be made (reduction in size, simpler cells, improvements in power consumption), then this could have a significant effect on the choice of pixel for liquid crystal SLMs.

### 3.6 Liquid Crystal over Silicon SLM Technologies

Table 3–1 presents a summary of liquid crystal SLM technology developed over the past 12 years at the University of Edinburgh.

<table>
<thead>
<tr>
<th>Year</th>
<th>SLM</th>
<th>Process</th>
<th>Pixel Size ($\mu m^2$)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1986</td>
<td>16x16 XNOR-SRAM</td>
<td>6$\mu$m NMOS</td>
<td>200x200</td>
<td>[63][64]</td>
</tr>
<tr>
<td>1988</td>
<td>50x50 XNOR-SRAM</td>
<td>1.5$\mu$m NMOS</td>
<td>74x74</td>
<td>[65][66]</td>
</tr>
<tr>
<td>1989</td>
<td>176x176 1T-DRAM</td>
<td>3$\mu$m CMOS</td>
<td>30x30</td>
<td>[54]</td>
</tr>
<tr>
<td>1993</td>
<td>256x256 XOR-SRAM</td>
<td>1.2$\mu$m CMOS</td>
<td>40x40</td>
<td>[67][50]</td>
</tr>
<tr>
<td>1996</td>
<td>512x512 1T-DRAM</td>
<td>1.2$\mu$m CMOS</td>
<td>20x20</td>
<td>[55]</td>
</tr>
<tr>
<td>1996</td>
<td>1024x768 1T-DRAM</td>
<td>0.7$\mu$m CMOS</td>
<td>12x12</td>
<td>[58]</td>
</tr>
</tbody>
</table>

Table 3–1: Summary Information on Liquid Crystal over Silicon SLMs.

It can be seen that there has been a significant increase in pixel count, with a reduction in process geometry and pixel area.

These trends (larger array devices with smaller pixels), are being mirrored elsewhere, for example, a 640x512 DRAM device [68], and a 1280x1024 DRAM device [69].

Pixel count is also affected by the maximum die (i.e. chip), size available for a given process. Again, this has been following an upwards trend.
3.7 Future Silicon CMOS Technology: Implications for LC SLMs

Silicon CMOS technology has been the main method of implementing VLSI circuitry for many years. Improvements to this technology are continuously being made and this will impact on future SLM devices.

3.7.1 Future Silicon Technology

Silicon CMOS technology is expected to be the dominant technology for the implementation of VLSI design for the foreseeable future [70]. Silicon CMOS technologies will have smaller feature sizes, larger die sizes, lower power consumption, and more conducting (metal) layers [71].

These metrics are summarised in Table 3-2.

<table>
<thead>
<tr>
<th>Year</th>
<th>Minimum Feature Size ($\mu$m)</th>
<th>1995</th>
<th>1998</th>
<th>2001</th>
<th>2004</th>
<th>2007</th>
<th>2010</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DRAM Cell ($\mu$m$^2$)</td>
<td>1.5</td>
<td>0.6</td>
<td>0.24</td>
<td>0.096</td>
<td>0.038</td>
<td>0.015</td>
</tr>
<tr>
<td></td>
<td>SRAM Cell ($\mu$m$^2$)</td>
<td>8</td>
<td>3.2</td>
<td>1.3</td>
<td>0.52</td>
<td>0.21</td>
<td>0.08</td>
</tr>
<tr>
<td></td>
<td>Number of Conducting Layers</td>
<td>4-5</td>
<td>5</td>
<td>5-6</td>
<td>6</td>
<td>6-7</td>
<td>7-8</td>
</tr>
<tr>
<td></td>
<td>Supply Voltage (V)</td>
<td>3.3</td>
<td>2.5</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>0.9</td>
</tr>
</tbody>
</table>

**Table 3-2: Summary of Future Trends for Silicon CMOS Technology.**

In addition to the metrics presented in Table 3-2, silicon fabrication houses are able to manufacture chips with an ever-increasing maximum die area. For example, AMS [72] manufactured the 256x256 XOR-SRAM on a die area of 14x14mm$^2$ in 1993. The fabrication house is now able to manufacture chips with an area of 20x20mm$^2$. 
Chapter 3. *Liquid Crystal over Silicon Spatial Light Modulators*

### 3.7.2 Future Liquid Crystal over Silicon SLMs

Table 3-1 presents trends in the development of Liquid Crystal over Silicon Spatial Light Modulators at the University of Edinburgh over the past 12 years (i.e. larger array devices with smaller pixels). These trends are mirrored elsewhere: larger array devices are being developed both in university research groups and in industry.

For example, DisplayTech [73] are currently developing a 1280x1024 DRAM LC SLM with a pixel pitch of 7.6\(\mu\)m [69].

The smaller process geometries and larger die areas will allow ultra-resolution devices to be designed, i.e. devices with a pixel count of over 2000x2000, and it is possible that the pixels used in these future devices could have a sub-micron area.

These “improvements” though, are not without their disadvantages for liquid-crystal devices. The reduction in supply voltages means lower driving voltages for the liquid crystal. This will have to be taken into consideration when designing devices and selecting liquid crystal mixtures to be used.

#### The Future of DRAM SLMs

Some previous large array SLM devices have been implemented using DRAM pixels (with all their attendant disadvantages), in order to attain a required pixel count. Improvements in SRAM pixel architecture (as detailed in this thesis), coupled with improvements in process technology, may make DRAM SLMs obsolete — except in a situation where many analogue voltage values require to be stored.

---

3Bearing in mind that the 1024x768 device listed in Table 3–1 was implemented on a 0.7\(\mu\)m process with a die area of approximately 17x17mm\(^2\).
It may be argued that DRAM devices will always provide smaller pixels than SRAM implementations; however, there will be a minimum size, below which pixels for LC SLMs cannot be implemented. This is due to two limiting factors:

1. Liquid Crystal switching occurs within domain walls. That is, molecules do not switch individually, but in groups. It is expected that below some physical limit, the domain will be too small to allow switching to occur [74].

2. Ferroelectric Liquid Crystals have a spontaneous polarisation value \( P_s \), measured in Coulombs/area (for example 1fC/\( \mu m^2 \)).

An SLM device may require a pixel size of 1\( \mu m \times 1\mu m \) in order to achieve a specified pixel count. This means the pixel ideally requires to store a charge of 2fC (using Equation 2.2), in order to switch the liquid crystal. For a +5V process the (DRAM) capacitance would — ideally — have to be 0.4fF, for a lower voltage process, the capacitance would have to be greater.

It may be impossible to design a DRAM cell with the given dimensions to have this capacitance since the parasitic capacitance values may not be high enough. SRAM cells do not require such consideration as charge is supplied from the \( V_{DD} \) and \( V_{SS} \) lines. And, a future 0.07\( \mu m \) process may allow SRAM pixels to be designed to 1\( \mu m \times 1\mu m \).

Therefore the original reasons for selecting DRAM pixels may no longer apply. In addition, ultra-resolution devices may require a slow refresh rate due to the numbers of pixels. Therefore it becomes even more advantageous to have devices that charge balance quickly over one clock cycle rather than having a full frame-inverse frame strategy.

The Future of SRAM SLMs

As discussed previously, SRAM pixels have often not been implemented in LC over Si SLMs as DRAM devices offer a higher pixel count. However, as discussed in the previous section, there will be a size limit, below which, DRAM pixels
cannot be implemented. If Silicon technology continues to progress as expected, it is possible that SRAM pixels could be designed having a lower area than the DRAM “limit”, and so, DRAM devices may no longer be required.

3.8 Summary

Static RAM pixels demonstrate advantages over DRAM pixels. They provide better driving voltages for the liquid crystal and enable SLM devices to have a higher frame rate.

Spatial Light Modulators are becoming larger i.e. more pixels in larger array sizes, with many — much smaller — pixels, and are now being manufactured on sub-micron processes.

This has important implications for device yield, power consumption of individual pixels, the size of individual pixels, and the complexity of individual pixels.

This chapter has also discussed the expected trends in Silicon process technology and their potential impact on Liquid Crystal SLMs.

It is desirable to improve charge-balancing SRAM pixels in terms of area, complexity, and power consumption so that they can be used in preference to DRAM pixels in future SLM devices.

4Unless — as mentioned previously — many analogue values require to be stored on-pixel.
Chapter 4

Novel Load-and-Display SRAM Pixels for LC-over-Si SLMs

So far, this thesis has presented background material relating to Liquid Crystal Spatial Light Modulators, and discussed the importance of load-and-display SRAM pixels in such devices. This chapter details the work carried out to improve such SRAM pixels in terms of size, power consumption, and circuit complexity.

4.1 Introduction

As detailed in the previous chapter, existing SRAM pixels that incorporate charge-balancing circuitry use an XOR or XNOR circuit. Such a circuit has disadvantages as the circuitry can be large and complex. Transistors used in such designs may have to be lengthened (i.e. made long-channel), in order to increase their resistance and limit switching current spikes [75].

It can also be seen from the pixel schematic (Figure 3-8), that the drive scheme to the pixel mirror is unequal: in one half-cycle, the mirror is driven by the CLOCK busline passing through a transmission gate; in the other half-cycle, the mirror is driven by a signal supplied by the SRAM outputs.
The operation of such XOR devices is actually very simple: the pixel circuitry merely has to produce a LO-HI transition if the cell is storing a '1', and a HI-LO transition if the cell is storing a '0', or vice-versa (see Figures 3–8, 3–9).

A simpler method of implementing this output toggle was developed, one that would improve pixel characteristics.

### 4.2 New Pixel Circuitry

All that is required of the charge-balancing circuitry is to toggle or switch the pixel output LO-HI or HI-LO depending on the value stored. Therefore a simple switching architecture that does this is required (see Figure 4–1).

![Figure 4–1: The Novel Charge-Balancing SRAM Pixel Architecture.](image)

The circuit operates as follows:

When $\phi_1$ is enabled, S1 closes, and the OUTPUT node takes the value of LATCHBAR. When $\phi_2$ is enabled, S2 closes, and the OUTPUT node takes the value of LATCH.
Therefore if the SRAM is storing a ‘1’, the **OUTPUT** node goes LO-HI; if the cell is storing a ‘0’, the node goes HI-LO as required ¹.

In a CMOS context, the switches are replaced with transmission gates or pass transistors, and the $\phi_1$ and $\phi_2$ signals are replaced with some form of clocking signal or signals.

The use of the enhancement mode PMOS and/or NMOS transistor as switches is a crucial part of the new pixel circuitry, an explanation of the such transistors in switching applications is given in the following section.

### 4.2.1 MOS Switches

An NMOS enhancement mode transistor will be “ON”, i.e. it will have a low impedance conducting channel between its source and drain, when there is a positive voltage drop ($V_{gs}$), between its gate and source. This voltage drop must be greater than some threshold voltage ($V_{th,NMOS}$), of say $+1V$. Above this threshold, the transistor is on, below the threshold the transistor is effectively off (see Figure 4-2).

![NMOS and PMOS Transistors](image)

**Figure 4-2:** NMOS and PMOS Transistors. The diagram shows the labelling of the source, gate, and drain nodes.

¹In fact it does not matter whether it is a ‘1’ or a ‘0’ that causes the output LO-HI, as long as the output toggles alternate ways with either state.
PMOS devices operate in a similar way, except that the gate-source voltage $V_{gs}$ has to be negative, and less than some threshold of say $-1V$.

The threshold voltage is defined by [76]:

$$V_{th} = V_{t(0)} + \gamma(\sqrt{V_{sb} + 2\phi_F} - \sqrt{2\phi_F})$$

(4.1)

Where $V_{t(0)}$ is the threshold voltage when $V_{sb} = 0$, and the other terms describe the modulation of this threshold voltage by the body effect: $V_{sb}$ is the substrate voltage with respect to the transistor source, $\phi_F$ is a constant for a given process, and $\gamma$ is the body effect coefficient — a constant that describes the substrate bias effect.

That is, the threshold voltage is not constant: as $V_{sb}$ increases, $V_{th}$ increases.

**NMOS Pass Transistor Switches**

NMOS transistors can be used as switches, however they are not ideal [77] [78]. Consider the following.

![NMOS Transistor Switch](image)

**Figure 4–3:** An NMOS transistor switch.
A signal has to be routed from the transistor drain to the transistor source. The transistor is switched by a signal on the gate. Initially the source is at logic 0 (0V).

If the transistor is switching a logic 0, then when the gate goes HI, the logic 0 at the drain is routed to the source (since \( V_{gs} > +1V \)). However if the transistor is switching a logic 1 — say +5V — then the source capacitor \(^2\) starts to charge up from 0V. Once this capacitor reaches +4V, \( V_{gs} \) no longer exceeds the threshold voltage and the transistor turns off.

Therefore an NMOS transistor is good at transmitting LO logic signals but attenuates logic HIs.

**PMOS Pass Transistor Switches**

PMOS transistor switches operate in a similar way [79].

Again, a signal has to be routed from the transistor drain to the source; initially the source is at logic 1 (see Figure 4–4).

\(^2\)This capacitor may be formed from parasitics in the circuit, or by the gate of another transistor.
If the transistor is switching a logic 1, then when the gate goes LO, the logic 1 at the drain is routed to the source, since $V_{gs} < +1V$. However if the transistor is switching a logic 0 then the source capacitor starts to discharge down from +5V. Once this capacitor reaches +1V, $V_{gs}$ is no longer lower than the threshold voltage and the transistor turns off.

Therefore a PMOS transistor is good at transmitting HI logic signals but attenuates logic LOs.

Transmission Gates

In order to solve the problem of logic signal attenuation, a PMOS and NMOS transistor can be connected in parallel [80] [81].

![Figure 4-5: The Transmission Gate Structure and Symbol.](image)

Such a circuit is known as a transmission gate (see Figure 4-5). The circuit acts as a good switch, but is larger in area than a single pass transistor and also requires complementary switching signals. That is, since both transistors have to be ON simultaneously; when a HI SWITCH signal is used to turn the NMOS transistor on, a LO signal is required to turn the PMOS transistor on.

There are many different combinations of transmission gates, pass transistors, and clocking strategies that can be used in the new pixel circuits, several are discussed in the following sections.
4.2.2 10 Transistor SRAM Pixel

The 10 Transistor SRAM Pixel uses transmission gates to route the LATCH and LATCHBAR signals to the pixel mirror.

![Diagram of 10 Transistor SRAM Pixel](image)

The transmission gates ensure that good logic levels will propagate to the pixel mirror.

The pixel requires 10 transistors — the same number as the XOR design — and also requires a complementary clock signal. However, the transistors used in the transmission gate can be minimum-sized, unlike those used in the XOR circuitry, and — with careful layout — the extra clock line does not incur extra circuit size or complexity.

The circuit is data-loaded in the same way as a conventional SRAM cell. When CLOCK is HI, OUTPUT is LATCHBAR; when CLOCK is LO, OUTPUT is LATCH as required.

As with the XOR-SRAM, the Front Electrode can be set to $V_{DD}/2$ or to the CLOCK signal.
Chapter 4. Novel Load-and-Display SRAM Pixels for LC-over-Si SLMs

10 Transistor SRAM Pixel: Design Considerations

There are important operational features of this pixel that must be considered at the design stage.

Current Spikes If — as in this case — a single-phase inverted clock signal is being used, then there will be a point when CLOCK is changing from HI to LO and, simultaneously, CLOCKBAR is changing from LO to HI (or vice-versa).

This means that both transmission gates will be partially on (see Figure 4–7).

![Figure 4-7: Current Spikes in the 10T Pixel caused by a single-phase inverted CLOCK Signal.](image)

Care must be taken to ensure that current spikes produced under these conditions are acceptable.
That is, CLOCK is a global signal, therefore if an array of 1000x1000 pixels are being clocked, and each pixel draws a switching current of 10μA, then this means a total switching current of 10 Amps could be drawn onto the chip.

To prevent this, transistors may have to be lengthened, or clock signals may have to be skewed (delayed) so that sections of the array switch at different times (see Figure 4-8).

In addition to the clocking current spikes, there are also transient current spikes that occur when loading the SRAM cell with a new value (i.e. when the inverter gates are switched). This feature of CMOS technology is well documented [62] and will not be discussed here.

Care must be taken to ensure that these spikes also are acceptable.

**Pixel Mirror Capacitance**  On each clock transition the SRAM cell is trying to drive the mirror to a different state. If the mirror capacitance is very large then there is a danger that the mirror may drive the SRAM cell instead. That is, charge will flow from the mirror back into the SRAM cell (see Figure 4-9), and cause it to erroneously change state.
Figure 4-9: Pixel circuit diagram showing the path for Mirror Charge leaking back into an SRAM Cell (dashed line).

Care must be taken to ensure that the mirror capacitance is acceptable and/or the SRAM inverters have sufficient drive capabilities.

4.2.3 8 Transistor 1 Clock SRAM Pixel

The Single Clock 8 Transistor Cell (8T1C), uses pass transistors to route the LATCH and LATCHBAR signals to the pixel mirror.
A single clock line can be used as the pass transistors are of complementary types. Again these transistors can be minimum-sized.

8 Transistor 1 Clock SRAM Pixel: Design Considerations

The Single Clock 8 transistor design requires the same current spike and mirror capacitance considerations as the 10 transistor pixel, in addition, the clock switching strategy must be altered.

Clock Switching Strategies  As mentioned previously, NMOS transistors are poor at switching HI logic levels and PMOS transistors are poor at switching logic LOs. Therefore if the pixel is storing a logic ‘1’, the voltages routed to the output node will be attenuated.

Since transmission gates have been discarded in order to reduce the pixel area and use only one busline, another approach is required in order to maintain good voltage levels at the pixel mirror.
The maximum voltage that can be routed through an NMOS transistor is given by:

\[ V_{\text{OUT}} = V_g - V_{\text{thNMOS}} \]  \hspace{1cm} (4.2)

Where \( V_{\text{OUT}} \) is the voltage routed from the transistor drain to its source, \( V_g \) is the voltage on the transistor gate, and \( V_{\text{thNMOS}} \) is the threshold voltage of the transistor.

So, in order to switch a logic 1 of say +5V, with a threshold (\( V_{\text{t(0)}} \)) of +1V, the gate voltage would have to be +6V i.e. \( V_{DD} + V_{\text{thNMOS}} \).

Similarly for PMOS transistors, the gate voltage may have to be −1V i.e. \( V_{SS} + V_{\text{thPMOS}} \), where the threshold voltage is −1V, and \( V_{SS} \) is at Ground (0V).

In reality, the supply voltages may have to be set outwith these values due to the body effect.

Therefore the \( \text{CLOCK}^* \) signal will have to be overdriven to voltages outwith the supply levels in order to maintain signal levels (the front electrode can be set to \( V_{DD}/2 \) or toggle between \( V_{DD} \) and \( V_{SS} \) as normal).

### 4.2.4 8 Transistor 2 Clock SRAM Pixel

This pixel design — the 8T2C (see Figure 4-11) — also uses 8 transistors, however two NMOS transistors are used to switch the SRAM outputs.

\(^3\)Neglecting the body effect for simplicity.
This means that two (complementary) clock signals are required, but this can simplify the switching strategy.

8 Transistor 2 Clock SRAM Pixel: Design Considerations

The current spike and mirror capacitance design considerations required for the 8 Transistor 2 Clock pixel are the same as those required for the 10 transistor pixel, though it has advantages over the 8 Transistor Single Clock pixel.

Clock Switching Strategies  Since two NMOS transistors are being used, the CLOCK* signal only has to switch between $V_{SS}$ and $V_{DD} + V_{th_{NMOS}}$ — this can be easier to implement than the switching required for the single clock design.

Another switching strategy would be to set the chip power supply to $V_{SS}$ and $V_{DD} + V_{th_{NMOS}}$. Then to toggle the front electrode between $V_{SS}$ and $V_{DD}$ as normal. This will give "normal" voltage swings across the pixel mirror without having to design circuitry to overdrive the clock.
Chapter 4. Novel Load-and-Display SRAM Pixels for LC-over-Si SLMs

It is also feasible to use two PMOS transistors to switch the SRAM outputs. To ensure good logic levels at OUTPUT, either the clock signals would switch between $V_{SS} + V_{thP莫斯}$ and $V_{DD}$, or the chip power supply could be set to $V_{DD}$ and $V_{SS} + V_{thPmos}$.

4.2.5 7 Transistor 1 Clock SRAM Pixel

This cell (Figure 4-12), uses the least amount of transistors and buslines.

![Diagram of 7 Transistor 1 Clock SRAM Pixel]

Figure 4-12: The 7 Transistor 1 Clock SRAM Pixel.

It is similar to the 8 Transistor 1 Clock pixel, but only uses a single data line to load the SRAM.

4.2.6 Other Pixel Implementations

Variations on the above designs have been detailed in a patent application [82] which has been filed and is included in Appendix A.

The variations include a 7 Transistor 2 Clock pixel, and use of NMOS transistors to load the SRAM cells. In fact, every possible combination of pass transistors
and transmission gates for loading the SRAM cell and switching the outputs is included. This is for completeness, since if a patent application is fully prosecuted it is not possible to add to the original.

4.2.7 Simulation Results and Comparisons

Some of the designs (and variations on them) detailed in the previous sections were laid out for the AMS 1.2µm, n-well, CMOS process. The designs were laid out using the Cadence CAD software, extracted, and simulated using HSPICE. At this stage they were not manufactured on silicon.

The AMS process was chosen as it was this process that was used to manufacture the 256x256 XOR-SRAM designed by Dwayne Burns in 1993 [67]. This enabled comparisons to be made between the XOR pixel used in that design and the novel devices.

The circuits were laid out as follows.

- XOR-SRAM Pixel.

  This pixel was used in the 256x256 XOR-SRAM SLM. The pixel allocates a 19x19µm area of metal for the pixel mirror. This is so that the SLM can be used without planarisation.

- Revised XOR-SRAM.

  This pixel does not use a pixel mirror pad, instead a via2 connection is used for the planarisation stage that will form the pixel mirror. This pixel was originally designed by Dwayne Burns as a replacement for the original XOR-SRAM pixel, and minor modifications were made by the author in order to meet process design rules. Unlike the original XOR pixel it is loaded via NMOS transistors.

- 10 Transistor Pixel.
This pixel — and all of the novel pixels — was laid out as having the same power, ground, busline and SRAM transistor dimensions as those used in the Revised XOR-SRAM design. This was done to try and make as fair a comparison as possible between designs. The novel pixels were also — like the Revised XOR-SRAM device — loaded via NMOS transistors.

- 8 Transistor 1 Clock Pixel.

- 8 Transistor 2 Clock Pixel.

This pixel was laid out as having complementary transistor types for loading the device (NMOS) and switching the SRAM outputs (PMOS). This minimised the pixel area.

The pixel was tested by varying the clock voltage used to clock the switching transistors, and then by varying the $V_{SS}$ supply in order to route good logic 0's to the mirror.

- 7 Transistor 1 Clock Pixel.

- 7 Transistor 2 Clock Pixel.

This pixel is identical to the 8 Transistor 2 Clock Pixel except that it is loaded using only one data line.

The new pixels used a quad structure (or similar), so that power lines and global buslines could be shared (see Figure 4-13).
The pixels’ performance metrics required careful thought.

The most obvious metric is the pixel area: it is desirable to make pixels as small as possible. The area was calculated by squaring the larger of the pixel’s length and breadth since pixels are not always quite square.

It is desirable to look at pixels’ maximum current drawn (i.e. current switching spikes) and power consumption. Initially it was thought that each pixel could be given an identical stimulus and the maximum current and average power values could be measured and compared. However this can give misleading results for several reasons.

Pixels may have small spikes when being loaded and large spikes when charge balancing (or vice versa). This means that current and power values may look favourable (depending on what test vectors are used), when in fact the pixel performance is poor overall. For example, a pixel could generate a 2mA current spike when being loaded with a logic 1, but have a charge balancing current spike
of 3pA. Therefore the average power could be very low if the test stimulus only has one load and many charge balance cycles.

The pixels were loaded with 1's and 0's and charge balanced over several clock cycles. In order to provide a more accurate picture of pixel performance, the maximum loading current was measured for each pixel. The average power associated with this spike was calculated and this was multiplied by the time over which the spike occurred. This gives the switching energy. This was done since the current/power spikes differ in duration between pixels and this makes it difficult to derive an accurate value for the average power.

The charge balancing maximum current spikes and average power were measured over one clock period as this is the same for all pixels.

The results are presented in Table 4–1.

<table>
<thead>
<tr>
<th>Pixel</th>
<th>Area (μm²)</th>
<th>$I_{MAX} (μA)$</th>
<th>Loading Energy (fJ)</th>
<th>Clocking $P_{AVE} (μW)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>256-XOR</td>
<td>1600</td>
<td>116.5</td>
<td>4636</td>
<td>21.14</td>
</tr>
<tr>
<td>Revised-XOR</td>
<td>961</td>
<td>135.08</td>
<td>5061</td>
<td>18.89</td>
</tr>
<tr>
<td>10 Transistor</td>
<td>942.49</td>
<td>112.95</td>
<td>5000</td>
<td>40.19</td>
</tr>
<tr>
<td>8T1C</td>
<td>846.81</td>
<td>123.47</td>
<td>4611</td>
<td>19.91</td>
</tr>
<tr>
<td>8T2C CK = -2.1V</td>
<td>823.69</td>
<td>106.1</td>
<td>4120</td>
<td>30.44</td>
</tr>
<tr>
<td>8T2C $V_{SS} = -1.55V$</td>
<td>199.2</td>
<td>38.46</td>
<td>33.90</td>
<td></td>
</tr>
<tr>
<td>7T1C</td>
<td>812.25</td>
<td>499.5</td>
<td>14288</td>
<td>19.88</td>
</tr>
<tr>
<td>7T2C CK = -2.1V</td>
<td>750.76</td>
<td>490.88</td>
<td>18696</td>
<td>30.44</td>
</tr>
<tr>
<td>7T2C $V_{SS} = -1.55V$</td>
<td>762.16</td>
<td>40.48</td>
<td>26272</td>
<td>33.89</td>
</tr>
</tbody>
</table>

Table 4–1: Simulation results for original and novel charge balancing load-and-display SRAM pixels.
All pixels showed a decrease in area and in the loading current, except for the 7 Transistor devices which have a large loading current, and for the 2 Clock devices when the supply voltage is increased.

The charge balancing current was higher in the novel devices, but this was expected due to the short-circuit between the SRAM outputs as the clock switched.

The table shows that the 10 Transistor and 8 Transistor devices give improvements over the XOR pixels in terms of area and maximum current spikes (this may mean that power lines could be reduced in size and so the pixel area could be further reduced). The 7 Transistor devices show a large improvement on pixel area over the XOR devices, but this is offset by the loading current spike.

The figures presented in Table 4–1 cannot be taken as absolute comparisons. This is because each SLM design will have its own requirements for pixel count, application area, silicon process to be used; this will affect the sizing of signal lines, transistors, and power lines.

Limiting Factors

It is feasible on the AMS process to lay out 8 transistors in an area of 20x20\(\mu m\). However the 8T1C is much larger than this since the pixel requires 2 power and 4 signal lines and it is not feasible to route these lines in an area of 20x20\(\mu m\). In fact, in order to lay out the 8T1C\(^4\) pixel in an area of 846\(\mu m^2\), the DATA and DATABAR lines were moved into metal3. Metal3 is not included as part of the AMS process — it is normally reserved for the the planarisation stage to increase the mirror size. In this case the increased pixel mirror would be formed from metal4.

This highlights the need for extra metal/routing layers in processes used to manufacture future SLM devices.

\(^4\)Also, the 8T2C, the 7T1C, and the 7T2C.
4.3 Summary

This chapter has described a new approach for implementing charge-balancing SRAM pixels by using switching circuitry at the SRAM outputs. Several different pixel designs have been discussed along with their design considerations. Simulation results have been presented which show the new pixels' advantages over existing circuitry.

Two test chips were designed in order to implement some of the preceding pixel designs (and other Smart Pixel circuitry). These will be discussed in the following chapters.
Chapter 5

The Implementation of Novel Charge-Balancing SRAM Pixels

A number of the pixel designs presented in the previous chapter were implemented on silicon devices. Some of these devices were subsequently assembled into SLMs. This chapter discusses the design and implementation of the SLMs.

5.1 Introduction

SRAM (and other Smart Pixel\(^1\)) circuitry was implemented on two separate chips (Xavier\(1\) and Wee Malkie). Each chip was fabricated using the Orbit 2\(\mu\)m, +5\(V\), double poly, double metal, n-well process; and the devices were manufactured through the MOSIS [83] service (this was due to the availability of silicon). Four Xavier\(1\), and twelve Wee Malkie chips were fabricated.

After fabrication, two of the Xavier\(1\) devices were assembled into SLMs and filled with a ferroelectric liquid crystal. This assembly was carried out by DisplayTech, Boulder, Colorado, U.S.A. [73]. Five of the Wee Malkie devices were assembled into SLMs by Boulder Non-linear Systems, Boulder, Colorado, U.S.A.

\(^1\)To be discussed in Chapter 7.
[84]. These devices were filled with a ferroelectric liquid crystal which could be used for analogue modulation.

The silicon process used and the SLM assembly did not allow high-quality pixels with bistable FLC to be implemented. It was not possible to planarise the devices, therefore minimum sized pixels could not be implemented as space had to be left for the pixel mirror. In addition, alignment layers could not be added to the SLMs, and the mirrors could not be polished as normally happens during in-house planarisation.

5.2 Xavier1

Xavier1 is a MOSIS “tinychip”. Its dimensions are 2.220x2.250mm. The chip has 40 I/O pads — 4 of which (the corner pads), are reserved for pad power and ground lines. The I/O pad structure is supplied by MOSIS. Users are advised not to alter this structure and to use the standard MOSIS I/O pad cells.

It was decided to implement only two novel SRAM pixel types on the tinychip. This was due to the restrictive dimensions and limiting pad count.

The circuit devices implemented were the 10 Transistor and 8 Transistor 1 Clock Pixels (see Figures 4-6, 4-10), except that the pass transistors used to load the SRAM cells were implemented as PMOS devices. This was because SRAM layouts used for the 256x256 XOR device designed by D.C. Burns (1993) could be quickly modified and implemented for this design.

These pixels were laid out as an 7x8 array of 10 Transistor devices, and a 2x4 and 2x2 array of 8 Transistor pixels. A larger array of 10 Transistor pixels was laid out as it was felt that the 10 Transistor pixels offered more immediate potential for implementation in large-array devices since the 8 Transistor pixels require special drive schemes. The two smaller arrays of 8 transistor devices were implemented with different clock driving schemes.
The pixel arrays implemented on Xavier1 used additional circuitry to facilitate loading and toggling the pixels: data shift registers, buffer registers, decoders and buffers. In addition, DisplayTech also required a large modulator test pad to be included on-chip. The test pad is a large mirror area connected directly to an I/O pad. This was to allow the company to make measurements of the liquid crystal contrast ratio and switching speed. However, DisplayTech did not ultimately make these measurements.

The layout of the chip can be seen in Figure 5-1.
Key

1. Clock buffers for 2x2 Array.
2. 2x2 Array.
3. Data Shift Register for 8x7 Array.
4. Data Buffer for 8x7 Array.
5. 8x7 Array.
6. Decoder for 8x7 Array.
7. 4x2 Array.
8. Capacitor for 4x2 Array.
9. Modulator Test Pad.
10. Other Circuitry.

Figure 5-1: The Xavier1 Chip. a.) shows a block diagram of the circuitry layout on the device — to scale. b.) shows a plot of the actual device.

DisplayTech specified layout requirements in addition to the inclusion of a test pad. These were to facilitate assembly of the SLM: a 400μm gap was to be left between the I/O pads and the pixel mirrors as the area of the cover glass was to be approximately 1.720x1.720mm² (see Figure 5–2).
Figure 5–2: The position of the Cover Glass on the Xavier1 Chip. The required gap between the cover glass and the bonding pads is indicated — not to scale.

The pixel mirrors had to be formed from areas of metal2 over metal1 over poly1 (i.e. they were to be the highest structures on the chip), and to have a pad cut made in order to expose the metal to the liquid crystal (see Figure 5–3).

Figure 5–3: The Pixel Mirror cross-section construction on the Xavier1 chip.

The company also provided figures for the expected liquid crystal performance
assuming a front electrode d.c. voltage of $+2.5V$ and mirror driving voltages of $0V$ and $+5V$.

10 Transistor Pixels

The 7x8 array uses row-column addressing similar to the 256x256 XOR SLM. The underlying logic for the data shift register, the data buffer, and the decoding circuitry is very similar to that used in the 256x256 device.

Data is loaded serially — using two non-overlapping clock signals — into and along the shift register. Once the shift register is full, the LOADLATCH signal is asserted. This loads the data buffer register from the shift register. Once the buffer register is loaded, the row in the pixel array is selected using the decoder circuitry. When SELECTENABLEBAR is HI, all the decoder outputs are disabled (i.e. no pixels can be loaded), when LO, the required output column is addressed by lines $S_0$, $S_1$, and $S_2$ (and their complements).

Circuitry showing the data and addressing can be seen in Figure 5–5.
Figure 5-5: The 7x8 Pixel Array Addressing and Data Loading. The figure shows one pixel with its associated address decoding and data loading circuit. The data loading circuit is clocked with PH1 and PH2 which are two-phase clocking signals.

HSPICE simulations were run in order to check the functionality of this cir-
circuitry. Simulations were also run on the pixel layout in order to check that current spikes were acceptable and that the (estimated) pixel mirror capacitance would not affect pixel operation.

5.2.2 8 Transistor 1 Clock Pixels

![Diagram of 8 Transistor 1 Clock SRAM Pixel](image)

**Figure 5–6:** The Xavier1 8 Transistor 1 Clock SRAM Pixel.

As mentioned before, the 8 Transistor pixel requires a special drive scheme in order to maintain good mirror voltage levels.

Simulations showed that drive voltages required to be approximately $+7\,V$ and $-3\,V$ in order to guarantee $0\,V$ and $+5\,V$ at the pixel mirror.

Two approaches were considered in order to generate the required $+7\,V$ and $-3\,V$, thus two pixel arrays were implemented.

The 2x4 Pixel Array — Drive Scheme 1

The first approach was to drive the pixels with $-3\,V$ and $+7\,V$ directly. That is, the CLOCK* signal would be generated off-chip and routed directly to the pixels without being buffered by protection circuitry on the chip I/O pads.
Electro-Static Discharge (ESD) protection circuitry is used on I/O pads to prevent damaging currents and voltages (i.e. those outwith the supply voltage), being routed to circuitry on the chip core.

Routing the CLOCK* signal directly to the chip core means that the pixel circuitry could be easily damaged when being handled. Since the voltage that can be routed to the transistor gate is given by:

\[
V = \frac{I \Delta t}{C_g}
\]  

(5.1)

And the voltage produced can be extremely high relative to the small current that may flow onto the chip from external sources if handled incorrectly.

For example, if \( I = 10\mu A \), and \( C_g = 0.03pF \), and \( \Delta t = 1\mu s \); then \( V = +330V \).

To lower the risk of damage, the CLOCK* line was deliberately loaded with a large RC value in order to limit current that could flow onto the chip if improperly handled.

This limits the maximum frequency of the CLOCK* signal, however optical testing and d.c. voltage probing can still be carried out.
The $2\times4$ pixel array utilises some of the addressing circuitry used by the $7\times8$ array.

This circuitry can be seen in Figure 5–8.

![Diagram](image)

**Figure 5–8:** $2\times4$ Pixel Array Data Loading and Addressing Circuitry.

The data word for the array is assembled using the same data shift and data buffer registers (and control sequence) as the $7\times8$ array — this was due to lack of space and I/O pads. For simplicity, the **ENABLEBAR** lines were implemented directly from 2 I/O pads (i.e. no decoding circuitry was used).

The control lines shown also have their complements routed to the circuitry where necessary.

**The $2\times2$ Pixel Array — Drive Scheme 2**

The second drive scheme generated the required voltages on-chip.

A $0V$, $+5V$ clocking signal would be input to the chip externally. This signal could pass through a standard I/O pad with its protection circuitry. The signal could then be fed through some on-chip circuitry to generate the required voltages.
In CMOS processes, signals outwith the normal operating voltages (in this case 0V and +5V), can be generated using transistors sited in wells that are tied to the appropriate voltage (see Figure 5-9).

![Pseudo Inverter Buffer Schematic](Image)

**Figure 5-9:** A Pseudo Inverter Buffer Schematic. $V_{IN}$, $V_{DD}$ and $V_{SS}$ can be set such that the voltage routed to the output can be $+7V$ or $-3V$.

In a twin-well process this arrangement can be easily implemented. However in a single-well process — such as the n-well Orbit — this is not straightforward as there are no p-wells, only a global p-substrate at 0V (the $+7V$ signal can be easily generated using an appropriate n-well).

It was decided to implement a very simple circuit that would be capable of generating the necessary voltage levels (under certain circumstances).

The circuit is a pseudo inverter buffer with the same schematic as in Figure 5-9. As the process supports n-wells, the $+7V$ signal can be generated in a straightforward fashion. The $-3V$ signal cannot, as there is no unique p-well.

In order to generate the $-3V$ on-chip, a p-well was synthesised by creating an n-well ring around a small area of the p-substrate. This small area is tied to the required $-3V$ and shielded (see Figure 5-10).
Current will flow in the substrate between the two areas of different potential (see Figure 5-11), but it should be small and not have an adverse effect on the circuit or chip performance.

**Figure 5-10:** A Synthesised P-well Inverter. Substrate current will flow as there is a potential difference and a current path between the synthesised p-well area and the main substrate.

**Figure 5-11:** Current flow to a Synthesised P-well. The diagram shows an overhead view of the current model as it flows into the synthesised p-well from the surrounding substrate.
This current flow is difficult to model accurately as the charge carriers may follow a complex path and the depth of the n-well must be considered (i.e. current will travel down through the substrate then up into the synthesised p-well). For simplicity in current calculations, current was modelled as passing through the four polygon areas in a horizontal fashion, and the substrate sheet resistance value was used in calculations.

The resistance of one polygon section is shown to be:

\[ R = 2R_\square \cdot (\ln b - \ln a) , \quad (5.2) \]

if the dotted lines bisect the right-angle corner at 45° (see Appendix B and Figure 5-12).

Figure 5-12: Resistance estimation of a polygon segment. Values \( a \) and \( b \) are the distances to the start and end of the polygon segment respectively, from the centre (origin) line that bisects the inner synthetic p-well area.

Where \( R_\square \) is the sheet resistance of the relevant material, and \( a \) and \( b \) are the inner and outer section distances.
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The total resistance of the structure will be the resistance of each polygon section evaluated in parallel (this assumes that the current distribution is equal all around the structure).

Using a sheet value of $2643 \Omega/\square$ for the substrate, and $a_1=33\mu m$ $a_2=42.5\mu m$, $b_1=71\mu m$ and $b_2=80.5\mu m$; the total resistance is $920\Omega$.

This gives an expected d.c. substrate current of $5.4mA^2$.

In order to limit this current, the length of the n-well could be increased. However the resistance only increases logarithmically with the length. That is, to increase the resistance by a factor of 10 would mean lengthening the n-well by a factor of 22,000 which is not realistic.

The calculated current can only be used as a guide: it has been calculated using assumptions of current behaviour in the substrate which may not be totally accurate. This estimation also neglects the effects of dynamic changes in the substrate due to the alteration of depletion regions around the n-well.

**Buffer Operation** The inverter buffer was implemented as it was felt that it was the simplest circuit that would allow generation of the required voltages given certain operating conditions.

What are these conditions?

If the buffer has an input of $0V$ or $+5V$ and the buffer power lines are set to $+7V$ and $-3V$ it does not follow that the output will take these values.

When the input to the buffer is $0V$ it is expected that the PMOS transistor will be ON and that the NMOS transistor will be OFF. However, if $V_{SS}$ falls below the threshold voltage of the NMOS transistor (say $+1V$), the NMOS transistor will be partially ON meaning that the output voltage may be attenuated slightly.

---

$^2$This value could inaccurate due to the assumptions made, and lack of knowledge on carrier behaviour in the substrate.
from $V_{DD}$. The converse is true for a $+5V$ input with $V_{DD}$ rising above $+6V$ (i.e. $V_{DD} - (V_{thPMOS})$).

The conditions are summarised in Table 5-1.

<table>
<thead>
<tr>
<th>Input</th>
<th>$V_{DD}$</th>
<th>$V_{SS}$</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>71</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>82</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-1</td>
<td>5-1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-2</td>
<td>4-2</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-3</td>
<td>3-3</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>-1</td>
<td>6-1</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>-2</td>
<td>5.5-0.5</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>-3</td>
<td>41</td>
<td></td>
</tr>
</tbody>
</table>

Table 5-1: Possible Input-Output Characteristics for a simple Level-Shifting Buffer. As the supply voltages vary, the output initially increases, but then decreases as the buffer acts as a potential divider.

It can be seen that if both supplies are varied at the same time, then, as they increase, the output voltages decreases because both transistors will be ON simultaneously, giving a power-to-ground current path. This current path acts as a voltage divider, and the resistance of the path (and output voltage) decreases as the magnitude of both supplies increases. However the buffer does — under certain circumstances — allow voltages of $-3V$ or $+7V$ to be sent to the pixel.

If $V_{DD}$ is to be routed to the output, $V_{SS}$ should be set to whatever value the input will take when LO (e.g. $0V$). If $V_{SS}$ is to be output, $V_{DD}$ should be set to the equivalent HI value of the input (e.g. $+5V$).

This was all that was required in order to assess pixel performance at this stage.

Note, these figures are only a guide as to what may happen as the supply voltages vary. They are not representative of the Orbit process.

The circuitry was laid as follows (see Figure 5-13).
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Figure 5–13: Circuitry used in the 2x2 Array. All signals are routed through an I/O pad. The \textbf{DATA} signal is inverted on the I/O pad, and the \textbf{CLOCK*} signal is buffered using the pseudo-inverter buffer.

Data is set on the \textbf{DATA} line which is routed to the left-hand column. The right-hand column is loaded with \textbf{DATABAR}, which is taken from the same I/O pad as \textbf{DATA} (the digital I/O pads buffer an input signal and also generate a complement). This approach was used as only one pad was available for data input and there were insufficient resources\(^3\) for the shift register approach used in the other arrays. Data is loaded to all pixels simultaneously i.e. only one \textbf{ENABLEBAR} signal is used for the whole array. Again this was due to insufficient resources.

\(^3\)I/O pads, die area and design time.
5.3 Wee Malkie

*Wee Malkie* is a MOSIS “smallchip”. Its dimensions are 4.2x6.6mm. Again — using MOSIS guidelines — it would normally have 40 I/O pads: ten on each side (although there is space for more) with 2 reserved for Pad Power and Ground.

Several more of the novel SRAM pixels were implemented on this chip as there was more silicon available (though the submission deadline was again imminent). In addition, some “smart” pixel circuitry was laid out (this will be discussed in Chapter 7).

Due to layout requirements specified by Boulder Non-linear Systems, one side of the chip had to be free from bonding pads. This required additional pads to be added to some sides (contrary to MOSIS recommendations) in order to implement the pixel circuitry.

Similarly to DisplayTech, BNS required pixel mirrors to be formed from areas of metal2 over metal1 over over poly1, with a pad cut on the metal2 area. Again, a clear distance was specified between bonding pads and pixel mirrors (400μm) to allow for the cover glass.

5.3.1 *Wee Malkie*: Circuit Layout and Design Issues

The novel SRAM circuitry implemented was as follows (see Figure 5–14):
Figure 5–14: The SRAM Pixel circuits implemented on the Wee Malkie chip.

Smaller arrays of these pixels were combined into a large 16x8 Array in order to share data and addressing lines.

The chip layout can be seen in Figure 5–15.
Chapter 5. The Implementation of Novel Charge-Balancing SRAM Pixels

Key

a.)
1 16x8 array of novel SRAM Pixels
2 Addressing circuitry for the 16x8 array
3 Clock buffer circuitry
4 Smart Pixel circuitry

Figure 5-15: The Wee Malkie Chip Layout of the SRAM pixels. a.) shows a block diagram of the SRAM circuitry layout on the device — to scale. b.) shows a plot of the device.

The 16x8 pixel array is made up of smaller arrays of pixels (see Figure 5-16 — again, complementary control signals are routed if required).
Chapter 5. The Implementation of Novel Charge-Balancing SRAM Pixels

Figure 5–16: The structure of the 16x8 Pixel Array. The diagram shows the clocking, addressing, and data loading circuitry. The complements of all the signals shown are routed to the circuitry if required.

- A 2x8 array of XOR pixels.
- A 2x8 array of 10 transistor pixels.
- A 4x8 array of 8 transistor 2 clock pixels.
- A 4x8 array of 9 transistor pixels.
- A 4x8 array of 7 transistor pixels.

The pixels share data and addressing lines. The 8 bit data word is made up in the same way as in Xavier1, however the addressing circuitry is not the same for each pixel sub-array — it differs for pixels being loaded with one data line since these devices are loaded using an NMOS transistor.

The individual pixel designs will now be discussed in more detail.
XOR Pixels

Figure 5-17: The *Wee Malkie* XOR-SRAM pixel with addressing lines.

These XOR pixels were based on the design used by Dwayne C. Burns in the 256x256 XOR SLM. They were included so that comparisons could be made between these and the novel devices.

These pixels are addressed by setting the ENABLEBAR line LO which is effected by selecting the appropriate column and enabling the SELECTBAR line.
10 Transistor Pixels

These devices were included in case there were difficulties in testing the pixels on *Xavier1*. The pixels are addressed in the same way as the XOR devices.

8 Transistor 2 Clock Pixels

These pixels are similar to the one described in Section 4.2.4 except that the SRAM outputs are routed to the mirror using PMOS transistors rather than NMOS. Unlike *Xavier1*, the *Wee Malkie* SLM did not include any facility to generate a clock voltage below Ground (i.e. the $-3V$ clock signal necessary to route a good logic ‘0’ to the pixel mirror). In order to test these pixels, the chip
power supply would be set to a value of $-2V$ or $-3V$ and $+5V$ to allow $0V$ to be routed to the mirror.

Addressing circuitry for this pixel was identical to that for the XOR pixels.

9 Transistor Pixels

These devices are identical to the 10 Transistor pixels except that they are loaded using one data line. They should toggle the same voltage values at the pixel mirror but require special data loading.

It is possible to design SRAM cells to be loaded with one data line — possibly by imbalancing the SRAM inverters or by increasing the width of the loading pass transistor. This is not ideal for SRAM pixels, since equal driving of the liquid crystal is desired, that is, both inverters should be identical; and it is desired to keep the SRAM cell as small as possible. Therefore loading of these devices is carried out by setting the ENABLE line to approximately $+7V$. This means
that the addressing circuitry differs from that used in the XOR, 10T, and 8T2C pixels. The **ENABLE** line is set HI to $+7V$ by using an inverter buffer with its PMOS transistor sited in a $+7V$ n-well.

7 Transistor 2 Clock Pixels

![Diagram](image_url)

**Figure 5–21:** The *Wee Malkie* 7 Transistor 2 Clock Pixel.

This pixel was implemented as the novel device with the lowest transistor count. The pixel is loaded in the same way as the 9 Transistor device. The pixel is clocked with a clocking signal that can be varied between $0V$ and some higher voltage which can be altered dynamically to ensure that a good logic ‘1’ is routed to the pixel mirror. Alternatively the chip power supply could be increased (with the clock toggling at $0V$ and $+5V$), above $+5V$ in order to route $+5V$ to the mirror.

5.4 Summary

This chapter has discussed the issues arising from the design and implementation of novel charge-balancing SRAM pixels on real silicon devices. The testing of the devices *Xavier1* and *Wee Malkie* will be discussed in Chapter 6.
Chapter 6

Novel SRAM Pixels: Testing and Results

This chapter discusses the testing of the two devices — Xavier1 and Wee Malkie — presented in Chapter 5.

6.1 Introduction

Both chips, Xavier1 and Wee Malkie, were tested electrically using a manual micro-electronic probe at a probe station, and optically, by viewing through a microscope. The microscope had a camera attachment which could be connected to a PC with a frame-grabber, this allowed pictures to be taken.

The chips were electrically driven using an interface circuit board. In the case of Xavier1, the board was self-contained i.e. all the necessary logic and switching was contained on the board. The interface board for Wee Malkie was much simpler: the control signals for Wee Malkie were generated using a PC with a programmable I/O card, the PC outputs were buffered using inverters on the interface board, then routed to the chip.

In both cases the board required several power supply voltage levels as voltages outwith the normal supply voltages of 0V and +5V had to be routed to the chip.
Also, both interface boards required a signal generator to provide a reference clock signal in order to generate clocking signals for the devices.

Due to lack of space under the microscope and at the probe station, the chips had to be mounted on a small piece of Veroboard which was connected to the main interface board using a long piece of ribbon cable. This limits the maximum clock frequency at which chips can be driven.

A switching board was also designed. This board could be inserted between the interface board and chip (see Figure 6-1).

**Figure 6-1:** The interface board setup for driving the test SLMs. The diagram is not to scale.

The switching board was designed so that signals from the interface to the chip could be left open-circuit or be multiplexed (see Figure 6-2) with a multiplexing signal.
Figure 6–2: The switching board circuit diagram for the SLM interfaces. The signal routed to the chip can be set open-circuit, to the interface output, or from some external GLOBALMUX source.

The switching board allowed signals to be set open-circuit, to the interface board signal, or set HI or LO (i.e. to the GLOBALMUX signal). This was extremely useful as it meant that signals to the chip could be set independently of the interface board. It also meant that sections of circuitry on the chips could be isolated for electrical testing. More specific examples of this will be given later.
6.2 Xavier1

Four chips were returned by MOSIS: two had been assembled into full SLMs by DisplayTech, the other two had been electrically packaged and bonded, though one had broken bonding wires and had been marked "bad" by MOSIS.

Views of the optical and electrical devices can be seen in Figure 6–3.

![Figure 6–3: The Xavier1 Optical and Electrical Devices. a.) shows the electrical device which has no cover glass and no liquid crystal. b.) shows the optical device: the bright area is the cover glass, underneath which lies the liquid crystal and the pixel circuitry.](image)

Note, the bonds to the centre of the chip on the electrical device a.) will be explained in the next section.

A self-contained interface board was constructed to drive and test Xavier1. The board's functionality was kept simple in order to allow a quick implementation: some data registers, switches for control signals (these signals were debounced if necessary), and simple internal control circuitry for the board itself.
Chapter 6. Novel SRAM Pixels: Testing and Results

The board required power voltage supply levels of $-3V$, $0V$, $+5V$, and $+7V$: these supply voltages, and data signals having these levels had to be routed to the chip.

6.2.1 XavierI: Electrical Testing

Initial testing of the optical devices gave no viable results. No pixels appeared to function although some liquid crystal switching was observed to take place over clock lines. After examination under a microscope it became apparent that the glue used to connect the front electrode wire to the cover glass was touching many of the bonding wires (some of which are power lines). Therefore there is a potential short circuit between (signal and power lines) and the front electrode; also, placing the wire may have dislodged some of the bonding wires (see Figure 6-4). There was also the possibility that the chips could have suffered from process mask errors and/or poor handling when being assembled.

![Glue Cover Glass](image.png)

**Figure 6-4:** Potential Short-circuit between the front electrode and bonding wires.

However, because pad cuts had been made across the pixel mirrors, it was thought that electrical probing of the devices may be viable. The difficulty with
this direct approach is that the point or head of an electrical probe is relatively large (e.g. 100x100μm), compared with the pixel mirror area (21.5x21.5μm), to be probed. Probing the mirrors themselves would not be feasible. Another approach was needed.

The damaged unassembled electrical chip was repaired by Mr. Alec Ruthven of the Edinburgh Microfabrication Facility (EMF), and electrical bonds were made from the modulator test pad and pixel mirrors to small metal pads that were glued to the chip package. These metal pads had a large area in comparison to the pixel mirrors and the probe head, and so could be probed easily (see Figure 6-5).

![Figure 6-5: A specially bonded Xavier1. Bonds have been made from circuitry (the modulator test pad and pixel mirrors), on the chip core to pads on glued onto the chip package.](image)

This bonding process is not straightforward as the bonding wire has a large diameter “blob” on the end that makes the connection. If the blob is too large it may not connect to the mirror (see Figure 6-6). Also, there is a danger of a short-circuit to adjacent pixels (see Figure 6-7).
Figure 6–6: Bonding to a small Pad-Cut. The diagram shows a cross-section of the bond and the pixel mirror to which the bond is made.

Figure 6–7: Bonding to a pixel on the 2x2 Array.
The bonded device was then electrically probed and tested.

Initial results showed that the modulator test pad (see Section 5.2.1) always showed $0V$ and did not vary with the signal driving it. This was due to a short circuit between the signal from the interface board driving the pad and ground. The chip layout was checked and no short was found in the on-chip circuitry, nor was the fault on the interface board. The fault therefore must be a mask error occurring during processing. This fault was common to all chips and further testing showed it to be replicated on other I/O pads.

The 2x2 and 2x4 arrays of 8 Transistor pixels functioned to some degree as expected, the 10 Transistor pixel gave $0V$ when probed and this value did not change with the clocking signal. It was thought that this was because the bond had not made contact with the pixel mirror.

Note, probing the pixels means that a minimum-sized inverter from the SRAM cell is driving a manual probe connected to a multimeter via a long wire. This is an extremely large load for such an inverter to drive. It means that this probing can only be used to read d.c. values from the pixel and is not feasible when clocking the pixel at high frequencies.

Since d.c. probing the device seemed feasible, the other unassembled chip was similarly bonded and detailed measurements were made.

The 7x8 Array (10 Transistor Pixels)

(The circuit diagram for this pixel can be seen in Figure 5-4.)

The interface board was designed to load an 8 bit data word into the on-chip data register. This data word could be set to any desired value. The appropriate column to be loaded could be selected by toggling switches on the board and then the necessary control signals could be set.

Control signals were debounced using R-S Latch circuitry.
Chapter 6. Novel SRAM Pixels: Testing and Results

The 7x8 array yielded no results from either of the electrical chips. When probed, the voltage remained at $0V$ regardless of the CLOCK signal (when clocked, the output should toggle). At this stage it was noted that the S0 I/O pad had the same error as the modulator test pad’s I/O pad (i.e. it was shorted to Ground). Further work with this circuitry gave no improvement and testing was abandoned since *Wee Malkie* contained similar 10 Transistor pixel devices.

This lack of results seemed most likely to be caused by a fault in the CLOCK line and/or an open-circuit between the bond and the pixel mirror.

2x4 Array (8 Transistor 1 Clock Pixels)

(The circuit diagram for this pixel can be seen in Figure 5-6.)

The 2x4 array uses the same method as the 7x8 array to form the data word (see Figure 5-8), although it is addressed without decoding circuitry: to load a column, the appropriate enablebar signal is switched.

The 2x4 array requires clocking signal with levels of $-3V$ and $+7V$. These levels were generated using two power supplies (see Figure 6-8). The $-3V$ and $+7V$ routed to the inverter chip can also be routed to Xavier1 to supply the on-chip clock inverter-buffer.
Results taken from both chips were inconclusive. Initially, the devices seemed to work as expected: when storing a ‘1’ value, and being clocked at 0V, +5V, the probed output toggled between approximately 0V and +4.12V. These values approached 0V and +5V as the digital levels of the clock signal were altered to -3V and +7V. These results were not reproducible after further testing.

The results degenerated with subsequent testing. At times the probe value was +2.6V and did not toggle with the clock signal; at other times, as the CLOCK* signal was varied to high voltages, coupling was observed between this high voltage and the chip supply. The pixel was also observed to toggle when the CLOCK* signal was disconnected from the array but active on other arrays — this could be caused by coupling through the capacitor used to protect the circuitry. Indeed, on other areas of the chip, clock lines were observed to

\[1\] The next section explains why voltages of 0V and +4.12V are expected during testing.
toggle if a clock signal was fed to the chip I/O pad when the chip had no power supplied to it.

Discounting other errors, it can be seen that the use of the large RC load on the CLOCK* line (see Figure 5-7), has an adverse effect on the circuitry and does not allow proper function to take place — signals are coupled onto the large capacitor from other sections of the chip.

Again, testing of this array was eventually abandoned since other 8 transistor pixels were available for test on the 2x2 array.

2x2 Array (8 Transistor 1 Clock Pixels)

(The circuit diagram for this pixel can be seen in Figure 5-6.)

The circuitry (see Figure 5-6), in the 2x2 array was such that when storing a ‘0’, good logic signals are expected at the output; and when storing a ‘1’, attenuated values are expected.

During testing it was noted that the pixel was often unable to drive the probe to the correct state when the ENABLEBAR line was not asserted. That is, the pixel occasionally flipped to an erroneous state when the clock toggled. This verifies the need for careful consideration of the load the pixel is trying to drive versus the driving capabilities of the SRAM inverters.

To test the performance of the pixel with varying CLOCK* voltage levels, a constant HI or LO signal was sent to the inverting buffer and its power supply was altered. To test the PMOS transistor, the pixel was loaded with a ‘1’, CLOCK* was set LO, and the VSS buffer signal was varied. To test the NMOS transistor, the pixel was loaded with a ‘1’, CLOCK* was set HI, and the VDD buffer signal was varied.

Initial results showed that the value routed via the NMOS transistor was initially +3.5V and increased as the inverter buffer VDD increased — this is as expected as it means that the CLOCK* voltage level is increasing. However,
the probed value through the PMOS transistor was 0V instead of the expected attenuated value of approximately +2V.

What causes this?

It was thought that probing the circuit was distorting the value, and, after discussion with colleagues, it seemed that the likely cause was that the voltmeter connected to the probe was discharging the node to ground through its internal resistance (see Figure 6–9).

Figure 6–9: Probe measurement distortion. Signals being measured at the probe point can be discharged through the voltmeter’s internal resistance.

That is, when the CLOCK* is switched from HI to LO, the output voltage will start to discharge from a HI value. This voltage should discharge to some attenuated value above 0V (the threshold of the PMOS transistor), however the remaining signal will discharge to ground through the voltmeter.

This feature was overcome by connecting the reference lead from the voltmeter to $V_{DD}$. This gave a probed value of $-3.33V$ (with the buffer $V_{SS}$ set to 0V), which equates to a threshold attenuation of $+1.67V$. This attenuation was expected as the PMOS transistor was being driven by a CLOCK* signal of 0V.

Probe results from one device are summarised in Table 6–1.
Table 6–1: Characteristics of an 8 Transistor Pixel in the 2x2 Array.

It can be seen that as the CLOCK* signal increases, the probed voltage values improve as expected.

The probed PMOS value does not quite reach $-5V$ — there could be several reasons for this:

- Distortion of the value by the method of measurement.
- System loss and substrate effects: the NMOS transistor in the CLOCK* inverter buffer is sited in a synthetic p-well and a loss current will be flowing in the substrate.

Substrate Current  In Section 5.2.2 an estimate of $920\Omega$ was made for the resistive path around the n-well guarding the synthetic p-well. A simple test was used in order to verify this estimate.

The buffer $V_{SS}$ voltage was varied and the current drawn by the supply was measured. Note, the input to the inverter buffer was set HI $(+5V$, as was the buffer $V_{DD}$), to turn the PMOS transistor off in order to prevent any current path through the circuitry. That is, the only current drawn should be that flowing in the substrate.
The following results were noted (see Table 6–2).

<table>
<thead>
<tr>
<th>$V_{SS}$</th>
<th>$I_{VSSLOW}$ mA</th>
<th>$R_{Substrate}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3</td>
<td>2.08</td>
<td>1442</td>
</tr>
<tr>
<td>-2.5</td>
<td>1.744</td>
<td>1434</td>
</tr>
<tr>
<td>-2</td>
<td>1.405</td>
<td>1423</td>
</tr>
<tr>
<td>-1.5</td>
<td>1.058</td>
<td>1418</td>
</tr>
<tr>
<td>-1</td>
<td>0.714</td>
<td>1401</td>
</tr>
<tr>
<td>-0.5</td>
<td>0.364</td>
<td>1374</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>0.5</td>
<td>-0.370</td>
<td>1351</td>
</tr>
<tr>
<td>1</td>
<td>-0.737</td>
<td>1357</td>
</tr>
<tr>
<td>1.5</td>
<td>-1.098</td>
<td>1366</td>
</tr>
<tr>
<td>2</td>
<td>-1.458</td>
<td>1372</td>
</tr>
<tr>
<td>2.5</td>
<td>-1.803</td>
<td>1387</td>
</tr>
<tr>
<td>3</td>
<td>-2.15</td>
<td>1395</td>
</tr>
</tbody>
</table>

Table 6–2: Substrate current and resistance caused by a synthetic p-well.

It can be seen that the measured resistance values are of the same order of magnitude as the calculated value. The calculated value is lower because it only considered a horizontal current path through the substrate underneath the n-well. Two other features should be highlighted. Firstly, the resistance value changes: it increases with the voltage drop. This is because one part of the depletion region around the n-well will increase with current flow creating a higher resistance. Secondly, the resistance values do not mirror one another around $V_{SS} = 0V$. This is because the other part of depletion region around the n-well will decrease as the potential in the synthetic p-well approaches $+5V$ (see Figure 6–10).
Figure 6–10: Depletion Region Variation in the silicon substrate. In a.) the depletion region pushes out right and down because of the potential difference between the synthetic p-well and the surrounding n-well and the substrate current flow. In b.) the depletion region is constant: the potential difference is constant all around the n-well and there is no substrate current flow. In c.) the depletion region pushes in on the right and out on the bottom. This is due to the reduced potential between the synthetic p-well and the n-well, and the substrate current.

6.2.2 Xavier1: Optical Testing

As discussed previously, initial optical testing of the Xavier1 devices yielded no results. The location of the front-electrode wire was such that some of the circuitry on the optical devices would be inoperable (i.e. the 7x8 Array and the 2x4 array), as the front-electrode wire was resting on power and control lines associated with that circuitry.

However, the pixels in the 2x2 array used separate power and control lines from those required by the 7x8 and 2x4 arrays. Using the switching board, the power and control lines affected by the front-electrode wire were switched out — left open-circuit.

Both optical devices were powered up and liquid crystal switching was observed to take place on one device only.

The clock voltage was varied by altering the $V_{DD}$ and $V_{SS}$ supplies to the clock inverter buffer and a slight variation of the liquid crystal grey-level was observed as expected (i.e. as the magnitude of the clock voltage increased, there was a slight analogue modulation of the liquid crystal).
However, the one operational optical device was of poor quality: there were defects in the liquid crystal, the cover glass and the pixel mirror areas were spotted; and overall, the quality of the liquid crystal was poor.

A picture of the optical 2x2 array can be seen in Figure 6–11. The grey-level image map has been altered to accentuate the difference between the liquid crystal ON and OFF state.

![Figure 6–11: The 2x2 Array on the operational Xavier1 optical device. The left-hand pixels store the complement of the right-hand pixels.](image)

It can be seen that the 8 Transistor Single Clock pixel is capable of driving liquid crystal as expected. However since only one device was operational, it was not possible to compare results between devices.

Although the optical results from Xavier1 are poor, the voltage values measured at the pixel mirror demonstrate full pixel functionality. Electrical results are of more importance in characterising pixels as it is the voltage on the pixel mirror that determines how the liquid crystal will behave.
6.3 \textit{Wee Malkie}

Twelve of these devices were manufactured and five of these were assembled into SLMs. The circuitry used to drive \textit{Wee Malkie} was simpler than that used to drive \textit{Xavierl}. This was because a host PC was used to generate the required control signals and data words — the interface board consisted mainly of inverters that buffered signals to and from the PC. This allowed greater flexibility in testing the chip and also decreased the time spent on designing and building the interface board.

6.3.1 Interface Board Design Issues

Synchronisation

The interface board is driven from a host PC with a digital I/O card and the I/O card can be programmed using ‘C’ code. When driving the chip, control signals have to be set or toggled for certain periods (or clock cycles). In order to do this, the PC has to synchronise with the global clock provided by the signal generator. This synchronisation was effected by having the PC wait for clock transitions before setting control lines, for example:

1. Wait for clock.
2. Set ENABLE HI.
3. Wait for clock.
4. Set ENABLE LO.

2 Phase Clock Generation

It was thought that the PC would generate the 2 phase clock signals required by the data shift registers. Code was written as follows:
1. Set PH1 LO, set PH2 LO.
2. Wait for clock.
3. Set PH1 HI, set PH2 LO.
4. Wait for clock.
5. Set PH1 LO, set PH2 LO.
6. Wait for clock.
7. Set PH1 LO, set PH2 HI.
8. Wait for clock.

This routine could be run as required to generate the necessary signals.

However this failed to operate the data shift registers. This was because the delay between PH1 switching LO and PH2 switching HI was too long (see Figure 6-12).

During this period all the transmission gates in the shift register are open, this means that any data stored in the register will decay (see Figure 6-13).
Figure 6–13: Signal decay in a shift register. Switch S1 is controlled by PH1 and S2 is controlled by PH2. When both signals are inactive, both switches are open, and the value stored in the register is subject to decay.

In order to prevent this, the delay time must be minimised. The computer could not switch signals quickly enough (i.e. the delay time was too great), so another method of generating PH1 and PH2 was needed.

The following circuit was used \(^2\) to generate the clocking signals.

Figure 6–14: 2 phase clock generating circuitry.

The delay between PH1 and PH2 switching is the signal delay time on path XY.

\(^2\)Based on [85]
6.3.2 Initial Results

As mentioned in the previous section, it was noted that the original method of implementing PH1 and PH2 was not satisfactory. This problem was discovered by viewing the optical devices — the signal lines routed in metal1 and metal2 caused liquid crystal switching even though there was passivation above the lines. This made it possible to determine where errors were occurring.

Viewing the optical devices showed switching of most pixels in the 16x8 array with the clocking signal. However, closer examination revealed a number of layout errors on the chip which reduced the functionality of the array.

In total, there were five errors on the chip. These took the form of short circuits, open circuits, and incorrect circuitry being laid out (a fuller discussion of why these errors occurred is given at the end of the chapter).

The errors were as follows:

- Open circuits on the clock buffer circuitry causing some clock lines to float HI.

  These errors only affected the 8T2C and the 7T2C pixels (see Figures 5–16 and 5–14), and meant that one of the clock signals on the pixels would be stuck at 1. This still allowed some testing to be carried out.

- Short circuits on the clock buffer circuitry.

  These did not adversely affect chip functionality. By altering the clock switching strategy, the problem could be solved.

- Open circuit on a data line.

  The data line from the I/O pad to the data shift register had a 4μm gap at one point. This meant that no new data could be loaded into the register.

- Incorrect circuitry laid out on the chip.
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This was the most serious error. An incorrect version of the data shift register was laid out. The layout was such that only the first bit of the register could be loaded and thus the first row in the array. All other stages were isolated from the 2 phase clocking lines required to load the register and also contained an internal short circuit.

- Short circuit on the Smart Pixel circuitry.

This prevented correct loading of a data register used to load a smart pixel array. This will be discussed in Chapter 7.

The scale and number of errors was both disappointing and frustrating. However, none were fatal to the chip operation: pixels still toggled (since they initialise to some random value on power-up), even though they could not be loaded with new programmable data. This allowed optical and electrical measurements to be made.

No remedial action could be taken on the optical devices since they had already been assembled into SLMs. Repairs were attempted on the electrical devices though, using a Focused Ion Beam (FIB) device which is sited in MIAC in the Department of Electrical Engineering at the University of Edinburgh.

Repair Action

The FIB is a device that can carry out high precision cutting on individual chips. A focused ion beam is used to cut through passivation and metal tracks in order to repair short circuits. The beam can also cut contacts onto metal tracks and the device can deposit metal in order to repair open circuits (see Figure 6-15).

3 A FIB200 model manufactured by FEI.
4 Microelectronic Imaging and Analysis Centre.
Chapter 6. Novel SRAM Pixels: Testing and Results

Figure 6-15: Chip repairs using a FIB. a.) shows an open-circuit error which is remedied by cutting vias on the metal tracks and then depositing metal. b.) shows a short-circuit error which is remedied by cutting through the appropriate metal tracks.

Two chips were worked on by Dr. Richard Langford and Mr. James Goodall. Attempts were made to correct all the errors except that of the incorrect circuitry as the magnitude of the task would have been too great, and it was not necessary, as access to one row would be sufficient to test loading the pixels. Measurements made from the two chips showed that some repairs had been unsuccessful: an open circuit on the clock buffer circuitry remained causing a stuck-at-1 fault on the 7T2C pixels. This will be discussed in the following sections.
6.3.3 Electrical Results

It was initially thought that the *Wee Malkie* devices would be bonded in a similar way to the *Xavier1* chips to allow electrical testing — one chip was bonded in this way.

This is not ideal though as it limits the scope for testing pixels: only the bonded devices can be tested, and only a small number of pixels can be bonded. Also, if the pixel yields no results, it is not clear whether this is caused by a fault in the pixel or the bond.

A novel way of probing the pixels was devised, this allowed any pixel in the array to be probed.

Normally, standard electrical probes have a large area probe head — too large to probe the pixel area of 21.5x21.5\(\mu\)m. A diabetic’s insulin syringe needle\(^5\), was used to probe the pixels. These needles are manufactured to be extremely fine, with a sharp, narrow point. The needle point is able to fit inside the pixel mirror area.

Needles were removed from plastic disposable syringes and mounted on the probe holders. Careful alignment of the probe and needle was still required in order to make a good electrical contact (see Figure 6–16).

\(^5\)A U100, 1ml Syringe, with a MICRO-FINE IV needle, manufactured by Becton Dickinson.
It was found that angling the needle at just below 45° with the barrel at right angles to the chip gave the best results when probing. The sharp needle point was also able to scrape away any aluminium oxide that had formed on the pixel mirror.

**XOR Pixels: Switching Results**

(See Figures 5–17 and 5–14 for the pixel circuit.)

These devices were observed to toggle with the clock signal. The probed value when the clock was HI was dependent on whether the pixel stored a ‘1’ or ‘0’. HSPICE simulations of the pixel driving an RC load verified this: that the probe was driven to different levels depending on the value stored in the pixel. When driving a small capacitive load, HSPICE simulations demonstrated that the pixel switched voltage values of 0V and +5V.
These results are summarised in Table 6-3.

<table>
<thead>
<tr>
<th>Data</th>
<th>CK0</th>
<th>CK1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>4.92</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>4.93</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>4.93</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 6-3: Switching values from XOR pixels on the Wee Malkie chips.

10 Transistor Pixels: Switching Results

(See Figures 5-18 and 5-14 for the pixel circuit.)

Probing these pixels yielded limited results. Only one chip demonstrated pixel switching, the others returned a probe value of 0V. The chip that showed switching gave values of 0V and +5V as expected. Further probing caused this switching to fail for no apparent reason. HSPICE simulations showed that the probe should have no effect on pixel operation.

This result is inexplicable: switching should occur as the optical devices show pixel switching, and other pixels (e.g. the XOR devices) using the same clock lines demonstrate switching (see Figure 6-17).

Figure 6-17: Optical Switching of the 10 Transistor Pixels on the Wee Malkie chip. a.) and b.) show switching of the same pixel over one clock period.
It was thought that perhaps the probe loading the pixel may cause large current spikes that may damage power supply and signal lines. An HSPICE simulation showed maximum current spikes of $120\mu A$ — well within the limits of the metal lines used in the pixel circuitry.

9 Transistor Pixels: Switching Results

(See Figures 5–20 and 5–14 for the pixel circuit.)

These devices — like the 10 Transistor pixels — yielded no results when probed. Again though, the optical devices demonstrated pixel switching as expected when the clocking signals were toggled (see Figure 6–18). This demonstrates pixel functionality.

![Image](image1.png)

Figure 6–18: Optical Switching of the 9 Transistor Pixels on the *Wee Malkie* chip. a.) and b.) show switching of the same pixel over one clock period.

8 Transistor 2 Clock Pixels: Switching Results

(See Figures 5–19 and 5–14 for the pixel circuit.)

The first two repaired devices were probed and performed as expected. With the multimeter reference line set at Ground, the switching values were $0V$ and $+5V$. When the reference line was set to $+5V$, the probed values were approximately $-3.33V$ and $0V$ as expected.
The ground supply of the chip was altered to see what effect this would have on the pixels. As the supply was lowered, the probed value of $-3.33V$ moved to $-5V$.

Results are summarised in Table 6-4.

<table>
<thead>
<tr>
<th>$VVss$</th>
<th>Probe</th>
<th>$VVss$</th>
<th>Probe</th>
<th>$VVss$</th>
<th>Probe</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-3.34</td>
<td>0</td>
<td>-3.36</td>
<td>0</td>
<td>-3.33</td>
</tr>
<tr>
<td>-0.5</td>
<td>-3.77</td>
<td>-0.5</td>
<td>-3.81</td>
<td>-0.5</td>
<td>-3.77</td>
</tr>
<tr>
<td>-1</td>
<td>-4.21</td>
<td>-1</td>
<td>-4.25</td>
<td>-1</td>
<td>-4.21</td>
</tr>
<tr>
<td>-1.5</td>
<td>-4.67</td>
<td>-1.5</td>
<td>-4.97</td>
<td>-1.5</td>
<td>-4.66</td>
</tr>
<tr>
<td><strong>-1.87</strong></td>
<td><strong>-5</strong></td>
<td><strong>-1.85</strong></td>
<td><strong>-5</strong></td>
<td><strong>-1.88</strong></td>
<td><strong>-5</strong></td>
</tr>
<tr>
<td>-2</td>
<td>-5.10</td>
<td>-2</td>
<td>-5.14</td>
<td>-2</td>
<td>-5.11</td>
</tr>
<tr>
<td>-2.5</td>
<td>-5.56</td>
<td>-2.5</td>
<td>-5.59</td>
<td>-2.5</td>
<td>-5.57</td>
</tr>
</tbody>
</table>

Table 6-4: Switching values from 8T2C pixels on the Wee Malkie chips. Columns A, B and C categorise results taken from different pixels.

The value of interest is the one where the probed output becomes $+5V$. This value was approximately $+1.87V$. This value is less than that required by the clocking voltage by Xavier1 to route a good logic 0 to the pixel output. The implications of these results will be discussed in the next section.

7 Transistor Pixels: Switching Results

(See Figures 5-21 and 5-14 for the pixel circuit.)

These devices toggled between approximately $+2.33V$ and $+3.33V$, or $0V$ and $+2.33V$, rather than the expected $0V$ and $+3.33V$.

This is due to the stuck at ‘1’ fault on one of the clock lines. This means that one of the NMOS transistors is permanently on (see Figure 6-19).
When the other clock signal also goes HI, there is a power to ground path between the SRAM outputs through both the switching transistors which acts as a voltage divider.

The fault remained even on the repaired devices. However, it was still possible to test the pixel by setting the clock such that the pixel output is at the +3.33V level, then altering the clock signal or the supply voltage.

Doing this verified the pixel's functionality: the +3.33V value increased as the clock signal and/or the supply voltage was increased.

These results are summarised in Tables 6-5 and 6-6.
Table 6–5: Switching values from the 7 Transistor 2 Clock pixels on the *Wee Malkie* chips using a varying clock signal. Columns A and B categorise results taken from different pixels.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLOCK</td>
<td>Probe</td>
</tr>
<tr>
<td>5</td>
<td>3.51</td>
</tr>
<tr>
<td>5.5</td>
<td>3.94</td>
</tr>
<tr>
<td>6</td>
<td>4.37</td>
</tr>
<tr>
<td>6.5</td>
<td>4.80</td>
</tr>
<tr>
<td>7</td>
<td>4.98</td>
</tr>
</tbody>
</table>

Table 6–6: Switching values from the 7 Transistor 2 Clock pixels on the *Wee Malkie* chips using a varying power supply. Columns A and B categorise results taken from different pixels.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Probe</td>
</tr>
<tr>
<td>5</td>
<td>3.51</td>
</tr>
<tr>
<td>5.5</td>
<td>3.88</td>
</tr>
<tr>
<td>6</td>
<td>4.35</td>
</tr>
<tr>
<td>6.5</td>
<td>4.80</td>
</tr>
<tr>
<td><strong>6.70</strong></td>
<td><strong>5</strong></td>
</tr>
<tr>
<td>7</td>
<td>5.25</td>
</tr>
</tbody>
</table>

These results demonstrate the pixel functionality and that the varying clock voltage must be higher than the varying power supply in order to route a good logic 1 to the pixel mirror.

The latter method of routing good logic levels to the pixel mirror (altering the power supply), is simpler than using an overdriven clock signal. However, it does have disadvantages.

Overall the chip may consume more power and have higher current spikes. This is because the whole chip is being driven at a voltage outwith the nominal supply voltage (as opposed to a method that only drives the clock lines at a greater voltage than the nominal supply).
Also, the settings for $V_{DD}$ or $V_{SS}$ to route $0V$ or $+5V$ are not the same between chips and may vary from pixel to pixel on chips (Tables 6-4 and 6-6 show a difference of up to $0.3V$ in the required voltage setting).

Therefore if this method is to be used, some form of calibration may be required for each chip, since the power setting must be accurate.

Using an overdriven clock though, any clock voltage greater than a certain level (e.g. $+7V$), is guaranteed to route the required voltage level to the pixel mirror. Implementing an overdriven clock on silicon may require more design, but gives better operation overall.

7 Transistor and 9 Transistor Pixel Loading

As discussed previously, probing the 9 Transistor devices yielded no results, therefore only the 7 Transistor pixels could be tested.

The repaired devices still exhibited the stuck-at-1 clock fault. This meant that pixels switched between $0V$ and approximately $+2.33V$, or $+3.33V \rightarrow +5V$ (depending on the clocking signal) and $+2.33V$.

In order to test loading these pixels, the clock was set so that the mirror voltage was either HI or LO (i.e. not at the short circuit voltage), and then the pixel was loaded.

With all (i.e. the clock and decoder) voltages set to the power supply ($+5V$), there was no alteration of the mirror voltage when the loading sequence was carried out. As the decoder voltage was increased (to approximately $+7.5V$), it was possible to switch the pixel from storing a ‘1’ to a ‘0’ as desired. However, attempting to switch state from ‘0’ to ‘1’ did not prove possible even when the voltage of the $ENABLE$ signal was increased to over $+9V$.

It was felt that, once again, the probe may be affecting the circuit’s operation. Therefore, the pixel was set to store a ‘0’, the probe was removed from the pixel mirror, and the loading sequence initiated. When the mirror was subsequently probed, the voltage level was ‘1’ as expected.
6.3.4 Optical Results

A visual examination of the optical devices demonstrated pixel functionality: pixels switched with the clocking signal, and altering the clocking voltage and power supply changed the pixel response as expected.

It was thought that it may be possible to obtain more quantitative results than those of visual inspection by capturing images using the PC frame grabber and then calculating mean grey-level values for pixels.

Pixel Analysis

The analysis was carried out as follows.

Two images of each pixel sub-array were captured — one image for each clock state. A pixel was selected from these images and highlighted with a template using the “xfig” computer package.

The single pixel could then be processed i.e. its mean grey-level value was calculated (see Figure 6–20).

This process was very time-consuming as images had to be converted between several image formats and the pixels of interest had to be manually selected and highlighted.
Images were grabbed from several optical devices and clock signal strengths and supply voltages were varied when appropriate. Only one of the optical devices was of sufficient quality to provide good images for processing. These are summarised below:
Chapter 6. Novel SRAM Pixels: Testing and Results

<table>
<thead>
<tr>
<th>Pixel</th>
<th>Mean Dark</th>
<th>Mean Light</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR</td>
<td>76.76</td>
<td>149.30</td>
</tr>
<tr>
<td>10T</td>
<td>70.04</td>
<td>168.64</td>
</tr>
<tr>
<td>9T</td>
<td>76.90</td>
<td>171.58</td>
</tr>
<tr>
<td>8T2C $V_{SS} = 0V$</td>
<td>87.68</td>
<td>166.20</td>
</tr>
<tr>
<td>8T2C $V_{SS} = -0.5V$</td>
<td>89.05</td>
<td>167.05</td>
</tr>
<tr>
<td>8T2C $V_{SS} = -1V$</td>
<td>89.28</td>
<td>170.69</td>
</tr>
<tr>
<td>8T2C $V_{SS} = -1.5V$</td>
<td>92.05</td>
<td>170.52</td>
</tr>
<tr>
<td>8T2C $V_{SS} = -2V$</td>
<td>96.73</td>
<td>169.06</td>
</tr>
<tr>
<td>8T2C $V_{SS} = -2.5V$</td>
<td>97.18</td>
<td>167.87</td>
</tr>
<tr>
<td>7T2C $CK = +5V$</td>
<td>71.32</td>
<td>140.31</td>
</tr>
<tr>
<td>7T2C $CK = +5.5V$</td>
<td>72.36</td>
<td>152.85 *</td>
</tr>
<tr>
<td>7T2C $CK = +6V$</td>
<td>77.41</td>
<td>148.81</td>
</tr>
<tr>
<td>7T2C $CK = +6.5V$</td>
<td>71.44</td>
<td>148.31</td>
</tr>
<tr>
<td>7T2C $CK = +7V$</td>
<td>70.33</td>
<td>148.04</td>
</tr>
<tr>
<td>7T2C $CK = +7.5V$</td>
<td>72.17</td>
<td>149.73</td>
</tr>
<tr>
<td>7T2C $V_{DD} = +5V$</td>
<td>71.32</td>
<td>140.31</td>
</tr>
<tr>
<td>7T2C $V_{DD} = +5.5V$</td>
<td>75.93</td>
<td>149.68</td>
</tr>
<tr>
<td>7T2C $V_{DD} = +6V$</td>
<td>73.41</td>
<td>151.99</td>
</tr>
<tr>
<td>7T2C $V_{DD} = +6.5V$</td>
<td>76.15</td>
<td>149.37</td>
</tr>
<tr>
<td>7T2C $V_{DD} = +7V$</td>
<td>79.70</td>
<td>151.19</td>
</tr>
<tr>
<td>7T2C $V_{DD} = +7.5V$</td>
<td>81.17</td>
<td>154.68</td>
</tr>
</tbody>
</table>

Table 6-7: Mean pixel grey-level values from *Wee Malkie*.

It can be seen that the average mean grey-level values vary with the clock signal. Also that the values for the XOR, 10T, and 9T pixels seem to show that the latter two pixels provide a better switching range than the XOR devices.

The 8T2C and 7T2C pixels show a variation in grey-level for the changing clock and power voltages. However it can be seen that there are some “glitches” in the readings, for example, the grey level value marked ‘*’ appears to be an error.

This happens for several reasons.

The frame-grabber is a non-ideal image source. When grabbing images, the grabber’s response is not time-invariant. That is, the same viewed image captured
at different times will give a different scan which may have a higher or lower mean grey-level.

This method of characterisation is not ideal for other reasons: individual pixels are prone to defects in the liquid crystal [86] [87]. Figure 6–21 shows what effect this can have on a pixel: the left hand pixel shows bars in the liquid crystal, the right hand pixel is of higher quality. Also, dirt on the cover glass can affect results.

![Pixel Mirror](image)

**Figure 6–21:** Liquid Crystal defects on a pixel mirror. The left hand pixel has defects (bars) on the liquid crystal. The right hand pixel is of higher quality, but shows a gradation in grey-level across the pixel.

Therefore, this method of measurement can be useful to show trends, but not for calculating absolute values.

Ultimately though, it is the mirror voltage that dictates the liquid crystal response and that can be more easily characterised, and has been, with less error for a number of pixels.
6.3.5 Errors

As discussed previously, the *Wee Malkie* device had several layout errors of varying severity. These errors occurred through a combination of circumstances (though ultimately the responsibility lies with the designer).

These are discussed below.

- Software.

  A major contributing factor to the chip errors are the limitations in the implementation of the Cadence software used for designing the chip, and the lack of knowledge the user had about the software.

  Cadence has a number of packages and tools, for example, schematic capture, layout versus schematic (LVS), and autoplace and route. These tools can be used to make a design flow proceed smoothly and to allow the designer to capture errors at critical stages. However, the author and his colleagues at design time were not aware of the existence of many of these tools, nor the knowledge of to use them.

  Proper use of schematic capture and LVS would most probably have caught the layout errors on *Wee Malkie*.

  This software knowledge gap is being addressed: the author and colleagues are writing documentation for the Cadence software that will make future chip designers aware of how a chip design flow should proceed, and what tools should be used by the designer at each stage [88].

  In addition, Cadence has a number of "features" that can cause errors if the designer is not aware of them. One of these may explain why incorrect circuitry was laid out.

  The 8 bit shift register and data latch buffer design was used in many parts of the chip: on the 16x8 array, and on the smart pixel arrays.
This design is made up in a hierarchical fashion: the register-buffer is made up from a register and a buffer, and the register is made up of 8 identical shifting cells.

These designs were copied around the chip for the 16x8 and the smart pixel arrays. The designs and their sub-designs had to be copied and renamed since the smart pixel arrays had different signal routing to the 16x8 array, and so the shift register for these arrays was laid out with different spacing between cells.

However, the design for the 16x8 array still contained components relating to the smart pixel array with a different signal routing, rather than its own unique set (see Figure 6-22).

![Hierarchical design structure in Cadence](image)

Figure 6–22: Hierarchical design structure in Cadence

This caused the errors in the data shift register.

- The CAD layout Display.

During the design process, the display window for the chip layout was set to have metall as a dark blue colour with the display window background as black. With hindsight, it would be better to set the metall layer as a distinct, bright colour, since gaps in a dark blue line on a black background are hard to detect.\(^6\)

\(^6\) All the layout errors were in metall.
• Finally, changes were made to the clock buffer circuitry at a very late stage in the design process and in such circumstances errors can be easily missed.

6.4 Summary

This chapter has discussed the testing procedure used on the XavierI and Wee Malkie SLM devices. Novel methods of testing the devices were devised in order to account for errors present on the chips. In spite of these errors, pixel functionality was demonstrated and behaviour was as expected as discussed in Chapter 5.
Chapter 7

Smart Pixels for Liquid Crystal SLMs

This chapter presents two novel smart SRAM pixels for implementation on liquid crystal over silicon SLMs. Design issues are highlighted and preliminary results are presented.

7.1 Introduction

So far, this thesis has presented novel designs for load-and-display SRAM pixels: pixels are loaded with some value that drives the liquid crystal into one of two states.

However, there is often a need for more complex, smart pixels to suit specific applications or perform specific functions.

S-SEED devices have been used in many smart pixel applications [15] [16] [14] since they offer a very high-data rate (i.e. switching speed). However, they cannot easily implement phase-modulation holograms [49]. Liquid Crystal devices — albeit with their slower switching speeds — can provide good phase modulation for holographic systems.

Two arrays of smart pixels were laid out on the Wee Malkie chip. These small pixel arrays demonstrated more complex functionality (and circuitry) than the novel devices presented in Chapters 4 and 5.
7.2 The X-Y Pixel Array

7.2.1 Introduction and Background

"It is... essential that a smart SLM is designed and fabricated... An array of 128x128 'interface' pixels with 8 bit memory store at each pixel will be designed."

The above quotation is taken from a SCIOS 1 proposal [89], to manufacture a new type of SLM device that would have several bits of memory at each pixel. The object of such a device was (when loaded with differing bit planes), to enable a new image to be displayed instantaneously by selecting the appropriate one from memory. This device would have applications as a holographic switcher since holograms can be used to switch optical data signals and a fast image update would enable fast data switching.

Holographic Switching Issues

The SCIOS proposal stated that the device would be used in a radix-2 holographic switching system. Some research was carried out to investigate the validity of this.

To switch \(N\) optical data channels holographically requires an SLM with a pixel count of at least \(8Nx8N\) pixels [90] (see Figure 7-1).

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1The Scottish Collaborative Initiative in Optoelectronic Sciences
Chapter 7. Smart Pixels for Liquid Crystal SLMs

If the above specification is used, then 8 bits of memory implies 8 switching patterns, that is 8 data switches. In a radix-2 context, (for example the 2D Fast Fourier Transform [91]), this implies using $2^8 = 256$ data channels. However, this would require a SLM with $2048 \times 2048$ pixels. A $128 \times 128$ device is, in theory, only capable of switching 16 channels holographically. With the radix-2, this means 4 switching patterns are required, and therefore only 4 bits of RAM are needed on the SLM. In order to switch many data channels, very high pixel count devices are required. However there is a limit to the number of pixels that can be incorporated onto a silicon die, and a trade-off between pixel size (and thus pixel count), and the number of RAM bits used.

In order to design an appropriate device, a $256 \times 256$ device with 5 bits of RAM would be more realistic. This is because such a device can holographically route 32 data channels, which matches the number of required radix-2 switches for 32 data points. However, such a device would be operating at its absolute limits (a small number of malfunctioning pixels may cause the device to fail), and would perhaps be too specialised thus of limited use in other applications.
Chapter 7. Smart Pixels for Liquid Crystal SLMs

### 7.2.2 A New SLM Device

The key issue in the original specification is that the image on the chip can be changed instantaneously (or at high speed), to allow rapid switching of optical data. There are other ways of implementing this, rather than storing values at each pixel.

Consider a large array SLM device (capable of switching many optical data channels). The SLM will be partitioned into sub-arrays with each sub-array containing a different switching pattern. The original optical data signal set will be duplicated onto each sub-array. However, all the arrays except the one selected will be blanked. For example, a 512x512 SLM could be partitioned into 4x256x256 arrays. Each array contains a different switching pattern. This effectively gives a 256x256 SLM with 4 bits of memory. The size of the sub-array can be determined dynamically, so the same device could be partitioned into 16x128x128, or 1024x64x64 (see Figure 7-2).

![Diagram of a novel SLM Switching Device](image)

**Input:**
- One source split into 4 beams.
- 512x512 SLM.

**Output**
- Split into 4x256x256 to generate 4 switching patterns.
- Only one array is enabled.
- All 4 switched sources will theoretically map to one detector array. However, only the selected one will be present.

**Figure 7-2:** A novel SLM Switching Device.

Such a device would require a novel addressing scheme and pixel design.
Addressing the SLM

The sub-arrays would be addressed in a similar way to a standard memory array (see Figure 7-3).

![Image of sub-array addressing on an X-Y Pixel Array]

**Figure 7-3:** Sub-array Addressing on an X-Y Pixel Array. The sub-array is addressed by ANDing the X and Y address lines.

An ‘X’-'Y' arrangement of select lines will be ANDed at each individual pixel to enable or disable that pixel’s output.

The New Pixel Design

The new pixel is based on a standard SRAM cell, but includes additional and novel, addressing and charge balancing circuitry (see Figure 7-4).
The pixel is based on a standard 6 transistor SRAM design. When the X_SELECT and Y_SELECT lines are enabled, the SRAM output is routed to the pixel mirror via the charge balancing transmission gate and inverter. The transmission gate and inverter route the value at node Z and its complement to the pixel mirror over one clock period as required for charge-balancing.

If either of the two control lines are not enabled, the SRAM output will be disabled and node Z will be set HI regardless of the value stored in the SRAM cell.

The new proposed device exhibited a number of advantages over the original design. These advantages included: a high pixel count — the original device has a proposed pixel count of 128x128 pixels, the new device would have a pixel count of 512x512 — and flexibility, as the new device can operate not only as a holographic switcher, but also as a high-resolution general-purpose SLM for other...
display or optical processing purposes (unlike the original proposed device which would only have provided a medium/low resolution image).

7.2.3 Implementation on Wee Malkie

An 8x8 Array of X-Y pixels was included on the Wee Malkie device for test purposes. Several design compromises were made due to I/O pad limitations. These will be discussed in Section 7.4.

7.3 The 4A Pixel

In addition to the binary SRAM pixels, an SRAM analogue pixel was laid out. The original concept for this pixel was Ian Underwood’s (of the Applied Optics Group, The University of Edinburgh).

The pixel is designed to route one of four analogue values to the pixel mirror (V0 or V1 or V2 or V3). Unlike DRAM pixels which can provide non-robust analogue values (i.e. voltages decay with time), this pixel provides a constant voltage signal (see Figure 7-5).
The pixel consists of two SRAM cells. The values stored in these cells route the appropriate voltage to the pixel mirror. This voltage is provided by a power supply and is not subject to decay. The right-hand SRAM cell contains a redundant inverter buffer. This is because the SRAM circuits had been designed as standard cells.

The voltages $V_0$, $V_1$, $V_2$ and $V_3$; can be set to any value. For the purposes of this device, it was expected that the voltage values would be set to gradated levels of the chip $V_{DD}$ supply. That is: $V_0 = 0V$, $V_1 = V_{DD}/3V$, $V_2 = 2V_{DD}/3$
and $V_3 = V_{DD}$. This provides an equal stepping between voltage levels over the range of the chip's $V_{DD}$ supply.

Note, unlike the other SRAM pixels presented in this thesis, the 4A pixel makes no attempt to automatically charge balance the liquid crystal. Due to time constraints, no attempt was made to include circuitry that could implement such a charge balance. To effect a charge balance, the front electrode would be set to $V_{DD}/2$, and the pixel loaded with its codeword (00, 01, 10, 11) and then its inverse (11, 10, 01, 00). This gives charge balancing as required.

This device has applications as a 4 phase level holographic switcher. Current SRAM liquid crystal SLMs can implement binary phase holograms [10]. That is, the phase of an incident light beam is modulated between 0 and $\pi$. However this produces many replicated, shifted images on the output plane. These replicated images are symmetrical about a central spot [92] [11]. This redundancy means that much of the light in the output plane is wasted.

By increasing the number of phase levels in a hologram, the output image can be made asymmetrical, and the efficiency of the hologram increased [93] [94] [95].

A 4x4 array of these pixels was included on the chip. Again, due to pad limitations, design compromises were made.
7.4 Layout Issues on *Wee Malkie*

The two smart pixel arrays were laid out as follows (see Figures 5–15 and 7–6).

![Diagram of X-Y and 4A Pixel Arrays](image)

**Figure 7-6:** The X-Y and 4A Pixel Arrays. The diagram shows the clocking, addressing, and data loading circuitry. The complements of all the signals shown are also routed to the circuitry if required.

7.4.1 Data Registers and Buffers

The circuitry for the registers is identical to that used in the *Xavier1* device (each register consists of a shifting register and a latch buffer register).

The registers were linked together in series since only one data line was available to load the arrays. This meant that in some cases long and complicated data words would have to shifted.
Chapter 7. Smart Pixels for Liquid Crystal SLMs

The X-Y registers were loaded by shifting a 16 bit data word and then enabling the LOADLATCHXY line. This does not load the buffer register in the data shift registers as they have a separate LOADLATCHDATA signal. This allows X-Y sub-arrays to be addressed (and changed) without perturbing the data already in the array (and vice-versa).

There was concern that the lines PH1 and PH2 from the I/O pads, used in the shift registers would be driving a large RC load (since the registers are connected in series). This may cause large current spikes when the signals switch. In order to reduce the RC load, inverter buffers were used in each shifting section to buffer these lines. At this point, time constraints prevented a detailed analysis of this signal behaviour, however a detailed analysis was subsequently carried out the results of which are contained in Appendix C.

7.4.2 Addressing

The arrays also shared the addressing lines S0, S1, S2 — since the 4A array has two SRAM cells per pixel and requires 8 SRAM cells to be addressed as does the X-Y array.
Figure 7-7: Addressing the X-Y and 4A Pixel Arrays. The pixel arrays share the NAND gate to save space. Unique addressing is achieved by each array having a separate SENBAR line.

To enable a line on the desired array, the required select S0, S1, S2 lines are enabled along with the appropriated SENBAR line.
7.5 Preliminary Testing and Results

Only brief testing was carried out on these pixels in order to verify basic functionality. Full characterisation and testing is being carried out by Mr. Jit Low as part of his 4th Year Honours Project in the Department of Electrical Engineering at the University of Edinburgh.

7.5.1 The X-Y Array

This optical devices were loaded with random images and liquid crystal switching was observed to take place. This shows that pixel-loading and liquid-crystal charge-balancing is effected.

The X and Y registers were then toggled off and on, and the pixel array was observed to flip between the the random image and the fully off state. This demonstrates the functionality of the X-Y addressing scheme (see Figure 7-8).

![Image](image.png)

**Figure 7-8:** Images of pixels from the 8x8 Pixel array on the *Wee Malkie* device. a.) shows an image displayed on the device with some pixels in the off state and some pixels in the on state. b.) shows the X-Y addressing lines disabled and all pixels are in the off state.
The electrical devices were also probed to ascertain what voltage levels were present at the pixel mirror. The probed values were 0V and +4.94V, +4.95V, and +4.96V over a range of pixels and chips.

These initial results show that the pixel array functions as expected: charge balancing occurs over one clock period as desired, and the X-Y address lines can be used to turn pixels “OFF”.

7.5.2 The 4A Array

On power up, the optical devices could be seen to display some random image. The pixels displayed greyscale values dependent on whatever state their component SRAM cells had initialised to.

The electrical devices were probed, and voltage values of 0V, +1.64V, +3.19V, +4.94V volts were noted (with $V_{DD} = +5V$). These values are as expected, since $V_0 = 0V$, $V_1 = V_{DD}/3$, $V_2 = 2V_{DD}/3$, $V_3 = V_{DD} = +5V$.

Loading the optical and electrical devices with new data did not show correct functionality and examination of the devices showed a layout error present on the data shift register. This error causes a short-circuit at the first bit position in the register and means that only the first column in the array can be loaded with programmable data.

In spite of this, it can be seen that the pixels demonstrate analogue switching of liquid crystal and that analogue voltages and liquid crystal states are observed at the mirror output (see Figure 7-9).
Figure 7-9: Images of a column of 4A pixels from the *Wee Malkie* device. This image was taken by Mr. Jit Low. a.) and c.) shows pixels in the $V_1$ voltage state, b.) shows a pixel in the $V_0$ voltage state, and d.) shows a pixel in the $V_3$ voltage state.

The layout error was rectified using the FIB and the corrected (electrical) devices are also being fully characterised by Mr. Low in addition to the original chips.

The error was most probably caused by some of the circuitry being moved on the final layout at a late stage in the design process after routing of the data and signal lines had taken place.

Again, had the methods of error detection and prevention described in Chapter 6 been used, the error would most probably have been discovered before the chip was sent off for fabrication.

7.6 Summary

Two smart pixel circuit designs for Liquid Crystal over Silicon Spatial Light Modulators have been presented. The motivation for these devices has been discussed, design issues have been highlighted and basic functionality has been demonstrated.
Chapter 8

Summary and Conclusions

This chapter summarises the work presented in this thesis and also suggests alternative approaches to those used by the author in designing, testing, and characterising future pixel devices.

8.1 Introduction

Liquid Crystal over Silicon Spatial Light Modulators are flexible, robust, devices with many application areas. This thesis has presented novel Static RAM pixel circuits for use in these devices.

8.2 Load-and-Display Pixels

The thesis has highlighted the need for robust pixel circuits that incorporate charge-balancing circuitry. Current pixel designs that have this functionality can be large, complex, and have high current and power requirements.

Novel circuits have been developed to implement SRAM load-and-display pixels that incorporate charge-balancing circuitry for liquid crystal over silicon SLMs.
These novel charge-balancing devices can have a lower area, be less complex, draw less current, and consume less power than current pixel implementations with the same functionality.

Table 4–1 characterises novel pixel layouts against a pixel layout (the XOR-SRAM), used in the 256x256 XOR-SRAM SLM.

Table 8–1 uses these results to give a projection of pixel count in a device¹ — with the same overall area as the 256x256 XOR-SRAM — that incorporates the new SRAM pixels

<table>
<thead>
<tr>
<th>Pixel</th>
<th>Pixel Area (μm²)</th>
<th>Pixel Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR-SRAM</td>
<td>1600</td>
<td>256x256 = 65,536</td>
</tr>
<tr>
<td>10T</td>
<td>942.49</td>
<td>333x333 = 110,889</td>
</tr>
<tr>
<td>8T1C</td>
<td>841.81</td>
<td>351x351 = 123,201</td>
</tr>
<tr>
<td>8T2C</td>
<td>823.69</td>
<td>356x356 = 126,736</td>
</tr>
<tr>
<td>7T1C</td>
<td>812.25</td>
<td>359x359 = 128,881</td>
</tr>
<tr>
<td>7T2C</td>
<td>750.76</td>
<td>373x373 = 139,129</td>
</tr>
</tbody>
</table>

Table 8–1: A comparison of areas and projected pixel count between a current load-and-display charge-balancing SRAM pixel and the novel devices.

It can be seen that using the novel pixel circuitry could dramatically increase the pixel count of an SLM.

The novel pixels were demonstrated to work as expected and can be used to implement improved SLM devices if used in preference to XOR-SRAM pixels.

The novel pixels though, can require special clocking schemes in order to drive the liquid crystal with the desired voltage levels.

¹Note that the pixel count will also depend on other factors, for example the pixel power consumption and current requirements.
Chapter 8. Summary and Conclusions

8.2.1 Clock Driving Schemes

In Chapter 5, a method of generating clock voltages outwith the power supply on a single-well process was described. The circuit used to implement the clocking signal was a simple inverting buffer which made use of a synthesised p-well to generate a \(-3V\) signal on-chip.

This circuit was demonstrated to work as expected, and the synthesised p-well approach offers potential for similar simple circuits to be used in n-well processes for test purposes.

8.2.2 Pixel Testing and Characterisation

Electrical and optical characterisation of the novel pixel devices was carried out. The optical characterisation was limited and time consuming; probing and measuring the pixel mirror voltages is a more accurate and useful way of evaluating a pixel’s performance.

The mirror voltage that determines how the liquid crystal will switch, however, at design-time it was not envisaged that the pixels would be probed so no effort was made to facilitate this.

In future test devices, if probing is to take place, the probe areas should be made larger in order to simplify the probing. However, probing the pixel can perturb the result, as discussed in Chapter 6. Therefore it would be advantageous to buffer the pixel output using some amplifying circuitry in order to prevent this, and to allow more accurate readings to be made (see Figure 8-1). In addition, the input impedance of the amplifier should be similar to that seen by the pixel when driving the liquid crystal.
In addition, it was seen that there were advantages to having sections of circuitry on a chip have their own power supply (as in the case of Xavier1). This means that if part of a chip is unusable, it can be switched out to prevent it interfering with the operational section.

8.3 Smart Pixel Devices

In Liquid Crystal over Silicon Spatial Light Modulators, the majority of devices utilise load-and-display pixels only, since these devices can provide for most of the application areas. However, this thesis has shown that there can be areas where more specialised devices are needed, and two smart pixel devices were discussed. Such devices can have a complex functionality and enable complex optical systems to be built.

8.4 Future Trends

The silicon CMOS industry expects to see a continued shrinkage of process geometry, an increase in die size, an increase in the number of metal layers, and a decrease in supply voltages over the next 12 years.

Many of these trends will aid the development of ultra-resolution SLM devices. However, consideration must also be given to the development of new liquid crystal mixes for silicon processes that will require lower supply voltages.
8.5 Mathematical Analysis

Appendices B and C present work carried out in the modelling of electrical characteristics of semi-conductors.

If signal behaviour is to be analysed and modelled accurately then there can be a need for the designer to make use of mathematical techniques and derive behaviour rather than blindly using simulation tools.

8.6 Concluding Remarks

Clearly this thesis has only presented novel pixel devices in a test environment.

The novel pixels though, will only exhibit their full potential in large array chips manufactured on modern, small geometry processes.

The Smart Pixel devices have potential applications in large holographic switching systems. In particular, the 4A pixel offers the possibility of easy implementation of stable 4 phase holographic switching systems.

The load-and-display circuits have the potential to replace the current XOR circuitry in future SRAM devices, and the SRAM devices in turn, the potential to become the mainstay in future ultra-resolution Liquid Crystal over Silicon Spatial Light Modulators.
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Appendix A

Author’s Publications

This appendix contains the author’s publications (which include a patent application submitted by the author to encompass the novel charge balancing load-and-display pixel circuits):


- Ian Underwood, John A Breslin, Dwayne C. Burns, Mike W G Snook, Anthony O’Hara, David G Vass. Advances in pixel design and wafer fabrication for liquid crystal over silicon SLMs. IEEE/LEOS Summer Topical Meeting on SLMs. 1996.


- J.A. Breslin, J.K. Low and Ian Underwood. Smart pixel with four-level amplitude or phase modulation. Accepted for presentation at the IEEE/LEOS
Appendix A. Author’s Publications

Summer Topical Meeting on Smart Pixels; to appear in the 1998 Digest of the IEEE/LEOS Summer Topical Meetings.
Patent Application

Novel Circuit Designs for Liquid Crystal over Silicon Spatial Light Modulator Pixels

John A. Breslin and Ian Underwood
Applied Optics Group,
Department of Electrical Engineering and Department of Physics,
The University of Edinburgh
10th February 1996
Patent Office Ref. No. 9602766.9
Appendix A. Author's Publications

Abstract

A new set of static logic circuit architectures for Liquid Crystal (LC), over silicon Spatial Light Modulator (SLM), devices is proposed. This new circuit set uses MOS transistors configured as pass transistors or transmission gates to generate a charge balancing waveform as required by the Liquid Crystal material. The new circuits mean that the pixel can: have a smaller area; have simpler connectivity; require fewer transistors; and require fewer buslines; than other pixel circuits implementing charge balancing waveforms by more conventional means.
This invention relates to a new set of circuits for Liquid Crystal over Silicon Spatial Light Modulator Pixels.

Introduction

Liquid crystal over silicon SLM devices have been produced for a number of years and have applications in displays, image processing, holography, optical correlators, and crossbar switches for telecommunications.

For digital pixels, each pixel can be in one of two states: on or off. This usually requires the pixel to store a logic value of '1' or '0'. Such storage can be effected using a Static RAM (SRAM) memory cell.

SRAM cells are larger in area than Dynamic RAM (DRAM) cells. They do not suffer from charge leakage and do not require refresh. This means that they can have better driving capabilities and can be more robust than their DRAM counterparts. They can also be viewed under constant, high intensity light. However, in order to charge balance the LC, extra circuitry is required. The charge balance requirement means that if the liquid crystal experiences a voltage $V$ for a time of $t$ seconds, it must be followed by a voltage of $-V$ for the same time period, otherwise the LC material degrades by electrochemical decomposition.

In current SRAM SLM devices\cite{1,p.64} an XOR gate can be used (see Figure 1, page 5), for charge balancing; or alternatively, an XNOR device can be used. In this application, the two are functionally equivalent.

The pixel can be loaded by setting ENABLEBAR to a low voltage state. Charge balance can be achieved by toggling the CLOCK signal. This produces the charge balancing differential voltage across the liquid crystal - if the cell is storing a '1' value (see $N^{th}$ Frame, Figure 2, page 6). If the SRAM is storing a '0' value, no charge balance is of course needed (see $N+1^{th}$ Frame, Figure 2, page 6).

Note that $V_{MIRROR}$ is measured from the XOR output to CLOCK, however it can also be measured in the opposite direction. The important point is that $V_{MIRROR}$ toggles between $+V_{dd}$ and $-V_{dd}$ over a frame when the SRAM cell stores a '1'.

This XOR circuitry can be implemented using an inverter and transmission gate (4 transistors) \cite{1,p.65}.

Novel Pixel Architecture Set

We propose a new SRAM pixel architecture set using pass transistors to replace the conventional XOR circuitry (see Figure 3, page 7).

Compared to the equivalent SRAM-XOR circuit, these architectures have the following advantages:

- Are smaller in area.
- Consume less power.
- Have simpler connectivity.
- Require fewer transistors (in some cases).
Appendix A. Author's Publications

- Require less buslines (in some cases).

The pixel architecture set implements a new way of toggling the SRAM output over a display period in order to charge balance the LC cell.

The diagram (see Figure 3, p. 7), shows a number of possible input and output stages all based on the use of pass transistors.

Various options exist - any input stage is compatible with any output stage.

<table>
<thead>
<tr>
<th>Input/Output Combinations</th>
</tr>
</thead>
<tbody>
<tr>
<td>aA, aB, aC, aD, aE, aF</td>
</tr>
<tr>
<td>bA, bB, bC, bD, bE, bF</td>
</tr>
<tr>
<td>cA, cB, cC, cD, cE, cF</td>
</tr>
<tr>
<td>dA, dB, dC, dD, dE, dF</td>
</tr>
<tr>
<td>eA, eB, eC, eD, eE, eF</td>
</tr>
</tbody>
</table>

Note:

- Some examples of how data can be written to the SRAM cell are given below:
  - Input\(_a\).
    Setting WRITE to a high voltage state.
  - Input\(_b\).
    Setting WRITEBAR to a low voltage state.
  - Input\(_c\).
    Setting WRITE to a high voltage and WRITEBAR to a low voltage state.
  - Input\(_d\).
    Setting WRITE to a high voltage state.
  - Input\(_e\).
    Setting WRITEBAR to a low voltage state.

- Some examples of how the output of the SRAM cell can be toggled across the pixel mirror are given below. In these cases, the FRONT ELECTRODE signal can be made equal to the CLOCK:
  - Output\(_A\).
    Setting CLOCK to a low voltage state and CLOCKBAR to a high voltage state. Then asserting CLOCK and CLOCKBAR to high and low voltage states respectively (at \(\pi\) radians out of phase, or preferably in a non-overlapping form).
  - Output\(_B\).
    Setting CLOCK to a low voltage state and CLOCKBAR to a high voltage state (at \(\pi\) radians out of phase, or preferably in a non-overlapping form). Then setting CLOCK and CLOCKBAR to high and low voltage states respectively (at \(\pi\) radians out of phase, or preferably in a non-overlapping form).
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- Output\(_C\).
  Toggling the CLOCK signal from a low to a high voltage state (or from high to low), over a frame.

- Output\(_D\).
  Setting CLOCK1 and CLOCK2 to a low voltage state; then asserting CLOCK1 and CLOCK2 to a high voltage state (with CLOCK2 lagging CLOCK1 to achieve non-overlapping clock signals).

- Output\(_E\).
  Setting CLOCK to a high voltage state and CLOCKBAR to a low voltage state at π radians out of phase.

- Output\(_F\).
  Setting CLOCK1 and CLOCK2 to a low voltage state, and CLOCK1BAR and CLOCK2BAR to a high voltage state. CLOCK1 is then asserted to a high voltage state, and CLOCK1BAR to a low voltage state (this is so that CLOCK1 does not overlap with CLOCK2BAR, and CLOCK1BAR does not overlap with CLOCK2), CLOCK2BAR is then asserted to a low voltage state, and CLOCK2 is asserted to a high voltage state.

- Naming of signal lines is strictly arbitrary.
- Any input stage is compatible with any output stage.
- The novel design set is valid with the clocking waveforms having a π (radian), phase shift from those described above. That is, over the display frame, the clock signals can run from low to high voltage states (with the clockbar signals running high to low), or vice versa.
- The control signals WRITE, WRITEBAR, CLOCK, CLOCKBAR, CLOCK1, CLOCK1BAR, CLOCK2, CLOCK2BAR, and FRONT ELECTRODE; can be supplied by buslines addressing an array of such devices. Alternatively, they can be supplied directly to, or generated on (with use of inverters for example), the pixel where appropriate.
- It is desirable to have fast switching of the liquid crystal. This requires LC material with a high spontaneous polarisation charge. This means the pixel mirror capacitance and driving voltages may have to be made large to allow the charge stored on the mirror to be large. The factors affecting mirror capacitance include: mirror area, plate separation, and liquid crystal permeativity.

When the SRAM cell is changing the charge stored on the pixel mirror, significant charge sharing may occur. Charge leaking from the mirror back into the SRAM cell may cause the cell to change its state. To counter this, the circuit must be designed so that the capacitance at nodes A and B must be such that charge sharing does not create an error state (the mirror capacitance may also be reduced). Alternatively, the pixel could be direct-driven from the D and/or DBAR lines.

References

Figure 1: XOR SRAM Pixel
Figure 2: Example Charge Balancing Waveforms
Figure 3: New SRAM Pixel Architecture Set
Advances in pixel design and wafer fabrication for liquid crystal over silicon SLMs

Ian Underwood, John A Breslin, Dwayne C Burns, Mike W G Snook, Antony O'Hara, David G Vass

The University of Edinburgh, Department of Electrical Engineering, Edinburgh, EH9 3JL, UK, Tel. (+44) 131-650-5652, email iu@ee.ed.ac.uk

INTRODUCTION

In the past few years, a shift in emphasis has occurred in the field of liquid crystal over silicon (LCOS) SLMs from the development of general purpose / proof of principle type devices to application oriented (if not application specific) devices [1]. The primary uses for LCOS technology currently appear to centre around the following non-coherent applications - displays for head mounting, projection etc - and the following coherent applications - dynamic holograms and correlators.

While a growing number of specialist smart-pixel LCOS SLMs are being reported, the majority of applications oriented smart-pixel LCOS devices designed to date are still electronically addressed and are based upon pixel circuits which are the direct equivalent of, or a variation on, their electronic memory counterpart [2]

- single transistor dynamic random access memory (1T DRAM)
- six transistor static random access memory (6T SRAM)

OBJECT

In this paper we will discuss advances in silicon fabrication technology which have allowed the production of LCOS SLMs with enhanced specification and performance. We will discuss advances in pixel circuit design and VLSI layout, for both DRAM and SRAM based pixels, which have resulted in higher pixel packing density and improved pixel performance. We will illustrate these advances using examples of our most recent SLM designs. The discussion will be based around the topics listed below.

Scaling of silicon technology
The availability of commercial fabrication processes with smaller minimum device dimensions and larger die sizes has allowed the design and production of devices with larger and larger pixel counts. This will continue into the future.

Increased Complexity Available from Silicon Technology
As the number of layers available on the silicon increases, it is possible to stack more of the pixel circuit vertically, thus decreasing the pixel area. For smart

A Now with Xilinx Development Corporation, Edinburgh
B Department of Physics, The University of Edinburgh
pixels, this is particularly true of the increasing number of interconnect layers which can take on further roles in addition to that of interconnect. Such roles include those of light blocking and acting as a ground plane to add shunt capacitance (see below).

**Custom Post Processing**
This allows the addition of further layers of interconnect, the planarization of top layers for an optically flat finish and the deposition of a final mirror layer which is optimised for optical quality rather than the usual current carrying capacity [3,4]. It further allows the deposition, pattern and etch of layers for liquid crystal alignment and liquid crystal layer spacing.

**DRAM Circuit Design**
Optimization of the performance of the single transistor pixel circuit requires that the full 3-D nature of the pixel be taken into detailed consideration. Liquid crystal switching speed and contrast ratio are enhanced by the maximization of the shunt capacitance (which is used to drive the liquid crystal) and by minimization of charge leakage from the shunt capacitor.

**SRAM and SRAM-XOR Circuit Design**
We previously reported on a 10T SRAM-XOR pixel circuit which has significant performance advantages over the 6T SRAM [5] for driving LC layers. We report here on a new SRAM-XOR circuit design which comprises as few as 8 transistors, allowing smaller area and reduced power dissipation in comparison with the 10T design.

**SUMMARY**
In summary we will consider firstly the requirements of the various applications and how they are best met by the available technology and secondly the prospects for continued advances in the medium term future.

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Appendix A. Author's Publications

Novel Static RAM Pixel Circuits for Liquid Crystal over Silicon Spatial Light Modulators
John A. Breslin and Ian Underwood
28th August 1996
Department of Electrical Engineering,
The University of Edinburgh
Mayfield Road,
Edinburgh, EH9 3JL,
SCOTLAND
+44 (0)131 650 5565 (Fax 650 6554)
John.Breslin@ee.ed.ac.uk

Abstract

We present two novel SRAM pixels for use in LC-over-Silicon SLMs. We describe the advantages of these devices, design issues, and driving schemes.
Appendix A. Author’s Publications

Novel Static RAM Pixel Circuits for Liquid Crystal over Silicon Spatial Light Modulators

John A. Breslin and Ian Underwood

28th August 1996
Department of Electrical Engineering,
The University of Edinburgh
Mayfield Road,
Edinburgh, EH9 3JL,
SCOTLAND
+44 (0)131 650 5565 (Fax 650 6554)
John.Breslin@ee.ed.ac.uk

Introduction

Liquid Crystal (LC) Spatial Light Modulators (SLMs) consist of an array of pixels manufactured on a Silicon backplane. Each pixel can, in binary devices, be on or off and thus stores a logic ‘1’ or ‘0’. This storage can be implemented using SRAM or DRAM cells.

A requirement of the LC is that it be charge balanced. That is, a voltage $+V$ for a time $t$ dropped across the LC, is normally followed by a voltage $-V$ for the same period $t$ [1]. In effect, the net d.c. voltage drop across the LC must be zero. This charge balancing process can be made simple by using an SRAM architecture with additional specialized circuitry.

Current SRAM Devices

Current SRAM “charge-balancing” pixels normally consist of 10 transistors: 2 pass transistors, 2 cross-coupled inverters, and a 4 transistor XOR (or XNOR), gate to allow the LC to be quickly and easily charge-balanced [2]. Other, simpler devices exist [3], but they rely on a frame inverse-frame loading strategy in order to implement the charge balance which is time-consuming. The inclusion of charge-balancing circuitry means that no extra frames require to be loaded onto the device.

The XOR function sets the pixel output LO-HI if the pixel stores a ‘1’, and HI-LO if the pixel stores a ‘0’ (on a HI-LO CLOCK transition). This ensures that the net d.c. voltage is zero across the pixel whether it is ON or OFF. However, the XOR circuitry is large, has a complex connectivity, is not ideal for driving the mirror, and suffers from dynamic power dissipation problems.

New SRAM Pixels

The new devices use transmission gates or pass transistors instead of the XOR gate, to switch the SRAM output LO-HI or HI-LO as required. Two devices are discussed (see Figure 2)

These new devices are: smaller, consume less power, have simpler connectivity, can have fewer transistors; than conventional SRAM-XOR circuits [4].
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Design Considerations

If, as in this case, one-phase, complementary clock signals are being used, there will be a point when the clock signal switches where LATCH and LATCHBAR are short-circuited. Simulations show that the maximum current drawn at this point is not damaging to the circuitry.

If the mirror capacitance is very large and the capacitances at nodes A and B are small, then when the SRAM cell tries to drive the mirror to a different state, charge could leak back from the mirror into the SRAM cell. This would cause the SRAM cell to change state erroneously. Care must be taken to ensure that the capacitance values associated with these nodes are ratioed properly.

In order to allow good switching of logic levels in the 8 transistor pixel, the pass transistors must be driven by a signal that switches between at least $V_{SS} - V_{th}$, and $V_{DD} + V_{th}$. This is to prevent attenuation of logic levels, as pass transistors are not ideal switches.

Implementation

Circuitry based on the above designs has been included on a test chip being fabricated on a 2µm, 5V, n-well process. Simulations show that to drive the 8 transistor devices properly requires voltages of $-3V$ and $+7V$. Two drive schemes were implemented to do this.

Drive Scheme 1

The first approach is to drive the transistors directly with a CLOCK signal of $-3V$ and $+7V$. This means that the standard pads with Electrostatic Discharge (ESD) protection circuitry cannot be used as they require 0V and 5V signal and supply lines. Therefore there is a danger of damaging the circuitry by generating large voltages on transistor gates whilst handling the chip [5, p.227]. In order to reduce this voltage, a large capacitance is placed at the input, in addition to resistors, to reduce potential current spikes. (see Figure 3).

Drive Scheme 2

The second approach is to build a buffer on the chip itself. The buffer takes a 0V, 5V input, and has
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a +7V, −3V output. This means that the CLOCK signal can be buffered via a standard input pad. However, the buffer requires a +7V n-well and a −3V p-well in order to operate. It is not possible to fabricate a p-well directly with the available process. However, a p-well can be synthesized by creating a n-well ring around a small area of the p-substrate. This small area is tied to the required −3V and heavily shielded (see Figure 4).

Conclusions

Two novel SRAM pixel circuits for use in Liquid Crystal over Silicon Spatial Light Modulators have been presented. These devices are smaller, less complex, have simpler connectivity, and consume less power than current devices. Any saving, no matter how small, in these attributes is extremely important given that future SLM devices will consist of well over one million pixels per die. Special considerations in design are important to ensure acceptable and error-free operation. Two drive schemes have been described that will allow these new pixels designs to be tested on a single-well process. Results from the Xavier1 test chip will allow these pixels to be incorporated onto very high resolution spatial light modulator devices. A patent application for these new circuits — and variations on them — has been sent to the UK Patent Office [4].

References


Abstract
In this paper, we present two novel Static RAM pixel designs for use in Liquid-Crystal-over-Silicon Spatial Light Modulators. Compared with existing designs, these new pixels have advantages in terms of circuit simplicity, circuit size, circuit connectivity, and power consumption. We discuss what considerations are required in the design of these pixels, why such considerations are important, and outline two schemes to drive the devices.

Introduction
Spatial Light Modulators (SLMs), consist of an array of pixels which, in binary devices, can be on or off (see Fig. 1).

Liquid Crystal (LC) devices use an LC material to modulate the amplitude and/or the phase of an incident light ray. There are several types of LC materials such as nematics and ferroelectrics [2]. For the purposes of this publication, ferroelectric liquid crystal will be discussed.

The devices are constructed by gluing the edges of a cover glass over a silicon die, on which an array of pixels is present. The inside of the cover glass is coated with a transparent electrode, and a gap is left between the electrode/glass and the surface of the die. This gap is filled with LC material.

One method of effecting amplitude modulation is as follows: Polarised light is presented to the pixel array. A voltage applied across the liquid crystal rotates the polarization of the light as it passes through the material. The “altered” light can be viewed through Polarizer B, the unaltered light cannot, and so the pixel appears dark (see Fig. 2).

These devices have applications in displays, holography and optical computing systems [1].

Figure 1. Spatial Light Modulator Pixel Array.

Figure 2. Amplitude Modulation using a LC SLM.

A requirement of liquid crystal materials is that they must be charge-balanced. This means that a voltage of
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$+V$ volts, applied for $t$ seconds, must be followed by a voltage of $-V$ volts, for $t$ seconds. That is, the net d.c. (i.e. time averaged) voltage across the material must be zero [3], otherwise the liquid crystal breaks down by electrochemical decomposition.

Each pixel in the array can be on or off, and thus has to store a logic '1' or '0' (for binary devices). This storage can be implemented using SRAM or DRAM cells.

**DRAM and SRAM Pixels**

DRAM cells are small and simple. However, they must be refreshed, suffer from photo-induced charge leakage, and may supply only a limited amount of charge to the mirror. To charge balance these devices may require a complex addressing scheme. This involves loading an image and then its inverse, possibly interspersed with blanking frames to turn the whole array on or off [4]. This lowers the frame rate of the device and means that the array has to be viewed under a pulsed light source.

SRAM cells are larger than DRAM. They require no refresh, are more robust, and provide better driving voltages for the pixel with an unlimited supply of charge (i.e. $V_{dd}$ and $V_{ss}$), via the SRAM cell — unlike the DRAM pixel which has a limited amount of charge stored in the DRAM capacitor. Also, SRAM cells can be viewed under a continuous light source. This is because specialised charge balancing circuitry can be incorporated directly onto the SRAM cell, and a complex addressing and driving scheme is not required (i.e. no inverse frame(s) require to be loaded). This in turn means that the device can have a higher frame rate.

**Current SRAM Technology**

Current charge-balancing SRAM pixels normally consist of a 10 transistor cell: Two pass transistors to allow data loading; two cross-coupled inverters to implement storage; and a XOR (or XNOR) gate to implement the charge balancing circuitry [5, p.64] [6] (see Fig. 3).

However, the internal XOR connectivity can be complex and the XOR circuitry may be large. This is because the transistors are lengthened in order to reduce current spikes when switching. The mirror is either driven by the CLOCK line through the transmission gate, or by a buffered (inverted) CLOCK. This means that the drive scheme is unequal as CLOCK is a global busline.

Charge balancing is effected by XORing the CLOCK signal — which is common to all pixels — with the stored data value (LATCH). This CLOCK signal is also present on the global Indium Tin Oxide (ITO), electrode. If the pixel is storing a '1', the mirror experiences a $+V_{dd}, -V_{dd}$, transition over one clock period. This will turn the pixel ON, and then implement the charge balance (the mirror having a 50% duty cycle). If the pixel is storing a '0', the XOR output is in phase with CLOCK, so the mirror will have a zero voltage drop and remain off. In each case, the net d.c. voltage across the mirror is zero (see Fig. 4) [5, pp.66-69]. Since the CLOCK line is common to all pixels, the charge balance occurs simultaneously across the whole array.

![Figure 3. Conventional XOR SRAM Pixel.](image)

![Figure 4. Charge Balancing Waveforms.](image)

The XOR gate is merely required to implement a LO-HI transition if the pixel is to be ON, and a HI-LO transition, if the pixel is to be OFF (or vice versa). Our new pixels use simpler techniques to do this.

**New Devices**

The new devices make use of transmission gates or pass transistors to switch the output of the SRAM cell LO-HI or HI-LO (or vice versa), as required. Two devices
Appendix A. Author's Publications

are discussed.

10 Transistor SRAM Pixel

This pixel contains 10 transistors. It consists of:

• A 6 transistor SRAM cell.
• 2 transmission gates switched by CLOCK and CLOCKBAR to toggle the SRAM outputs.
• When CLOCK is HI, OUTPUT is LATCH-BAR.
• When CLOCK is LO, OUTPUT is LATCH.

Advantages The transmission gate transistors can be minimum sized and the connectivity of the pixel is simpler — this leads to a saving in pixel area. Also, the mirror is driven directly by the SRAM outputs (via the transmission gates), so the drive scheme is balanced.

8 Transistor Pixel

This pixel contains 8 transistors. It consists of:

• A 6 transistor SRAM cell.
• 2 pass transistors switched by CLOCK*.
• When CLOCK* is HI, OUTPUT is LATCH-BAR.
• When CLOCK* is LO, OUTPUT is LATCH.

Advantages This pixel exhibits similar advantages to the 10 transistor design. In addition, it uses only 8 transistors, has an even simpler connectivity, and one less busline.

Comparisons

A comparison of pixel attributes, taken from the AMS 1.2μm, CMOS process, run at 5V, can be seen in Table 1.

Table 1. Pixel Attributes.

<table>
<thead>
<tr>
<th>Pixel</th>
<th>Area (μm²)</th>
<th>RMS Power (μW)</th>
<th>MAX (μA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>244-XOR¹</td>
<td>1683</td>
<td>60-1568</td>
<td>64-68</td>
</tr>
<tr>
<td>244-XOR (version)²</td>
<td>1420</td>
<td>195.79</td>
<td>184.1</td>
</tr>
<tr>
<td>10 Transistor</td>
<td>391</td>
<td>184.31</td>
<td>115.64</td>
</tr>
<tr>
<td>8 Transistor²</td>
<td>829</td>
<td>348.79</td>
<td>102.81</td>
</tr>
</tbody>
</table>

¹ This pixel was used in a 256x256 SRAM LC-SLM designed at the University of Edinburgh.
² This pixel is a redesign of the above.
³ Using an overridden CLOCK*.

With savings in pixel area and the continuing reduction in process geometries (IMEC [Belgium] offer 0.5μm CMOS and will soon offer 0.3μm [7]; IBM offers 0.18μm CMOS [8]), it is now feasible to produce Ultra-scale SRAM SLM devices, i.e. having resolutions of 1000x1000 to 2000x2000 pixels and above.

The new pixel designs can be further modified to reduce the number of transistors and buslines and/or change the transistor type(s) and configurations [9].

Design Considerations

Care must be taken in the design of the new pixel circuits shown in Figs. 5 and 6. Several important features must be considered.

Charge Sharing and Current Spikes
If, as in this case, one-phase, complementary clock signals are being used, there will be a point when the clock signal switches where both LATCH and LATCH-BAR are short-circuited. It is important to ensure that current spikes are acceptable under these conditions.

Pixel Mirror Capacitance
If the mirror capacitance is very large, and the capacitance at nodes A and B is small, then when the SRAM cell tries to drive the mirror to a different state, charge could leak back from the mirror into the SRAM cell. This would cause the SRAM cell to change state. That is, the mirror would drive the SRAM cell, rather than the SRAM cell driving the mirror. Care must be taken to ensure that the capacitance values associated with these nodes are rationed properly, and that the inverters have sufficient drive capability.

Simulations show that with a 30x30μm mirror, the capacitance of the mirror node would have to be over an
Appendix A. Author's Publications

order of magnitude above typical calculated values in order to effect this. That is, the mirror capacitance would have to be at least 1970 fF, when the typical value is actually 134.1 fF (with a node A capacitance of 13.29 fF).

Driving Schemes
The 8 transistor cell drives the mirror through a pmos or nmos transistor. In isolation, these devices are not ideal switches. A pmos transistor is able to switch a HI logic signal, but will attenuate a LO logic signal; when the gate voltage is LO. A nmos transistor will switch a LO signal, and attenuate a HI; when the gate voltage is HI [10, p.56]. The attenuation, for an nmos transistor, is as follows (see Fig. 7).

\[ V_c = V_n \text{ if } V_n < V_s - V_{th} \]

The threshold voltage \( V_{th} \), is not constant. It varies with the body effect [10, p.41]:

\[ V_{th} = V_{th}(0) + \gamma \left( V_{sub} + 2\phi_s - 2\phi_F \right) \]

Where, \( V_{sub} \) is the substrate voltage, \( \phi_F \) is a constant, \( V_{th}(0) \) is the threshold voltage when \( V_{sub} = 0 \), and \( \gamma \) is a constant that describes the substrate bias effect.

Therefore in order to allow good switching of logic levels in the 8 transistor pixel, the pass transistors must be driven by a \( CLOCK^* \) signal that switches between at least \( (V_{ss} - V_{th}) \), and \( (V_{dd} + V_{th}) \).

Implementation
Circuitry based on the above designs has been included on a test chip. The test chip (Xavier1), contains:

- an 8x7 array of 10 transistor SRAM cells.
- a 2x2 array of 8 transistor SRAM cells with drive scheme 1 (detailed below).
- a 2x2 array of 8 transistor SRAM cells with drive scheme 2 (detailed below).

The chip is being fabricated through MOSIS on the Orbit 2/µm, 5V, analogue, CMOS, n-well process.

Simulations show, that to drive the 8 transistor devices properly requires voltages of -3V and +7V. The latter can be generated using on-chip circuitry by shielding a n-well and strapping it to +7 volts. As it is not possible in an n-well process to create individual p-wells, a similar technique cannot be used to generate the required -3 volts.

Drive Scheme 1
The first approach is to drive the transistors directly with -3V and +7V. The \( CLOCK \) signal does not pass through any transistor circuitry on the chip. However, this means that the standard pads with Electrostatic Discharge (ESD), Protection circuitry cannot be used. Therefore there is a danger of damaging the circuitry when handling the chip. The actual voltage that could be generated at the transistor gate is given in Eq.3 [10, p.227]:

\[ V = \frac{I_{ds}}{C_{gs}} \]

The voltage produced can be extremely high relative to the small current that may flow onto the chip from external sources if handled incorrectly.

For example, if \( I_s = 10 \mu A \), and \( C_{gs} = 0.03 \mu F \), and \( \Delta t = 1 \mu s \); then \( V = 330 \) volts.

In order to reduce this voltage, the capacitance of the node is increased, and the line resistance is also increased to reduce the potential current (see Fig. 8). This approach limits the operational speed of the pixels, but will allow some testing and characterisation to be carried out.

Drive Scheme 2
The second approach is to build a buffer on the chip itself. The buffer takes a 0V, 5V input, and has a +7V, -3V output. This means that the \( CLOCK \) signal can be buffered via a standard input pad that contains ESD protection circuitry. However, the buffer requires a +7V n-well and a -3V p-well in order to operate (see Fig. 9).

It is not possible to fabricate a p-well directly with the available process. However, one can be synthesized by creating an n-well ring around a small area of the p-substrate. This small area is tied to the required -3 volts and heavily shielded (see Fig. 10).
Conclusions

It is desirable to use SRAM pixels in binary Liquid-Crystal-over-Silicon Spatial Light Modulators. On-pixel charge balancing circuitry allows devices to have a high frame rate.

We have presented two novel SRAM pixel circuits for use in LC SLMs. These devices exhibit several advantages over current designs.

Any saving in pixel area and current/power requirements can have a significant effect on the device resolution/size/performance/yield trade-off, especially in the design of very high resolution SLMs.

Acknowledgements

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References

Smart pixel with four-level amplitude or phase modulation

J.A. Breslin, J.K. Low and I. Underwood

The University of Edinburgh Department of Electronics and Electrical Engineering
The King's Buildings Mayfield Road Edinburgh EH9 3JL UK
Tel +44 131 650 5652 fax +44 131 650 6554 email i.underwood@ee.ed.ac.uk

We describe a pixel which allows four modulation levels to be selected in a layer of liquid crystal. We present results obtained on an array of prototype pixels on a test device.
Smart pixel with four-level amplitude or phase modulation

J.A. Breslin, J.K. Low and I. Underwood

The University of Edinburgh Department of Electronics and Electrical Engineering
The Kings Buildings Mayfield Road Edinburgh EH9 3JL UK
Tel +44 131 650 5652 fax +44 131 650 6554 email i.underwood@ee.ed.ac.uk

Introduction

The hybrid technology which utilizes a CMOS silicon active backplane to drive a thin layer of (nominally) binary-switching Ferroelectric Liquid Crystal (FLC) in order to produce a reflective Spatial Light Modulator (SLM) is now relatively mature [1]. The most commonly used pixel design uses only one active device - a MOS transistor configured as a digital switch to a storage capacitor. While suitable for most applications, leakage current from the pixel leading to a loss of voltage from the capacitor and a consequent perturbation of the state of the FLC is of concern [2] in coherent applications, e.g., when used as a programmable binary-phase holographic element. The use of static memory in the pixel has been demonstrated to alleviate the above problem [3].

In order to improve on the optical efficiency of a phase hologram produced by a binary SLM it is necessary to both (a) drive either multiple voltage levels or a continuously variable analog voltage into the pixel, and (b) utilize a fast switching analog-capable L.C. configuration. A single transistor can act as an analog switch but with the perturbation risk described above present.

In this paper we give an initial description of a pixel which allows one of four levels of (highly stable) voltage to be driven onto the pixel mirror thus allowing four levels of phase to be generated. This provides the advantages static memory drive with those of four level phase modulation, albeit at the expense of circuit complexity.

Pixel Circuit

Figure 1 shows a schematic diagram of the pixel circuit. The active circuitry comprises two main parts - a static digital two bit memory and a number of MOS pass transistors.

Figure 1  Schematic of pixel circuit
As well as the conventional $V_3 = V_{dd}$ and $V_0 = O V$ rails, an additional two voltage rails - $V_1$ and $V_2$ - are supplied to the pixel - $V_1$ at a nominal $V_{dd}/3$, $V_2$ at a nominal $2V_{dd}/3$. In practice, the intermediate voltages can be adjusted to compensate for nonlinearity in the response of the L.C.

The operation of the pixel is straightforward. The two bit word stored in the pixel memory determines which of the four voltage rails is shorted to the pixel mirror via the pass transistors as illustrated in Table 1.

<table>
<thead>
<tr>
<th>Memory</th>
<th>Transistors ON</th>
<th>$V$ mirror</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>$MN_5, MN_6, MN_7$</td>
<td>$V_0 (= 0V)$</td>
</tr>
<tr>
<td>0 1</td>
<td>$MN_5, MN_6, MN_8$</td>
<td>$V_1$</td>
</tr>
<tr>
<td>1 0</td>
<td>$MP_1, MP_2, MP_3$</td>
<td>$V_2$</td>
</tr>
<tr>
<td>1 1</td>
<td>$MP_1, MP_2, MP_4$</td>
<td>$V_3 (= V_{dd})$</td>
</tr>
</tbody>
</table>

Table 1 Routing of voltage to mirror as a function of word stored in memory

Implementation and initial optical characterization

An array of $4 \times 4$ of pixels has been implemented on a test chip. Due to an interconnect fault only one row of 4 pixels is addressable. Figure 2 shows a pattern programmed onto that row. Three of the four possible modulation states are visible. (The optics was configured to give amplitude modulation.)

Conclusions

FLC/VLSI SLMs offer a means of implementing programmable holograms. The pixel described here offers advantages over those previously used and has the potential to be implemented in a large array.

Acknowledgments

The authors acknowledge the COOP scheme through which the test chip was supplied and Boulder Nonlinear Systems which carried out the FLC cell fabrication and filling; the company also supplied. JAB is sponsored by the UK EPSRC and CRL Smectic Technology.

References

Appendix B

The Length/Width/Resistance Dependence of a Guard-Well

Consider a guard well placed around an area of substrate.

If the inner substrate is tied to a potential that differs from the outer then a current will flow between the two well areas.

This substrate current can be reduced by increasing the resistance between the two areas by increasing the length $L$ of the Guard-Well.

Figure B–1: An n-well guard in the silicon substrate.
How does the variation in length affect the resistance between the two substrate areas?

- Examine the shaded section of the Guard-Well.
Appendix B. The Length/Width/Resistance Dependence of a Guard-Well

Figure B-3: An n-well guard ring in co-ordinate space.

- Assume that the section is formed from small rectangular units of equal length \((dL)\), and width \(W\).

- The resistance of a rectangle is given by:

\[
R = R_0 \frac{L}{W} \tag{B.1}
\]

- Therefore:

\[
dR = R_0 \frac{dL}{W} \tag{B.2}
\]

But \(W\) can be written:

\[
W = \frac{2L}{m} \tag{B.3}
\]
Appendix B. The Length/Width/Resistance Dependence of a Guard-Well

Where \( m \) is the gradient of the dashed line in Figure B-3, and is dependent on whether the box's length is less than, equal to, or greater than its corresponding width.

So:

\[
dR = R_0 \frac{2dL}{mL}
\]  

Let \( dL \to 0 \), then total resistance \( R \) is given by:

\[
R = \frac{2R_0}{m} \int_a^b \frac{dL}{L}
\]  

B.5 becomes:

\[
R = \frac{2R_0}{m} (\ln b - \ln a)
\]

If we assume that the inner width \( a \) is kept constant (to its minimum value), then \( R \) can be written as:

\[
R = \frac{2R_0}{m} (\ln b - K)
\]

It can be seen from Equation B.8 that there is a logarithmic relationship between the length of the box and the resistance between the inner and outer areas. This is because the width of the outer area increases with the length.

This means that in order to increase the resistance by a factor of 10, the width would have to be increased by a factor of 22,000.

The mathematical derivation was verified by writing a short computer program. This program was given as input: the inner length of the well \( a \), the
Appendix B. The Length/Width/Resistance Dependence of a Guard-Well

outer length of the well \((b)\), and the number of sections or rectangles that the area had to be broken into \((n)\). As \(n \to \infty\), \(dW \to 0\).

Algorithm

1. set \(a = \text{InnerLength}\)

2. set \(b = \text{OuterLength}\)

3. set \(n = \text{no.ofsections}\)

4. set \(\text{length\_sum} = 0\)

5. for \(j = 0\) to \(n-1\) do

   \[
   \text{length\_sum} = \text{length\_sum} + \left( \frac{1}{a + 2 * (b - a) * j} \right) \tag{B.9}
   \]

   endfor

6. set

\[
R = R_\square \times \left( \frac{b - a}{n} \right) \times \text{length\_sum} \tag{B.10}
\]
Appendix C

Relating to Signal Behaviour in Conductors

C.1 Introduction

A length of conductor on a silicon chip is often approximated as an RC ladder network [100].

However this is just an approximation, it does not model signal behaviour exactly and may not suffice for accurate circuit analysis.

I wished to examine signal behaviour in a conducting signal wire (formed from metal1 or metal2 for example). I was specifically interested in modelling current spikes that would occur as digital signals switched along the wire \(^1\).

Digital signals that switch LO-HI or HI-LO contain high-frequency harmonics. The faster the switching time (the “sharper” the switching edges) - the higher the harmonics that the signal contains.

At high frequencies, capacitors have a low impedance. In a long conducting wire that is routed across a chip, a significant proportion of the capacitance associated with the wire can be between the wire and the substrate (which can be at Ground) — see Figure C-1).

\(^1\)As opposed to current spikes caused by charge sharing events and switching in logic circuitry.
Conducting Wire

Insulating Layer

Substrate

**Figure C-1:** A Conducting Wire over a Silicon Substrate.

When a signal switches along the wire, the wire may sink a large current spike from the signal source.

When laying out signal lines it is important to assess what currents the lines are expected to carry. Chip manufacturers will quote values for conducting metal lines in a silicon process, for example metal1: 0.5mA/μm at d.c. , and 25mA/μm for transient peaks (spikes).

This means that the current capacity of metal1 is 0.5/25mA/μm i.e. if you expect a signal line to route 5mA of d.c. current, then it has to be 10μm wide, or if the wire is to experience current spikes of 100mA, then it would have to be at least 4μm wide.

However, increasing the width of a metal line in a silicon process whilst increasing the current it can carry also lowers its resistance and increases its capacitance. This will actually increase the current that flows in the line. Therefore it is important to ensure that this increase in current is less than the current capacity of the wire.

I wished to find out what determined the maximum current flow in a conducting wire that is dominated by RC effects. For simplicity a step input was assumed and the wire was left as an open-circuit at its receiving end.
C.2 Current in a simple RC Network

A simple RC network can be modelled as follows.

This network can be described by the following differential equation.

\[ v_i(t) = i(t)R + \frac{1}{C}\int i(t)dt \quad (C.1) \]

Taking Laplace Transforms (and neglecting initial conditions):

\[ V_i = I(s)R + \frac{1}{C}\frac{I(s)}{s} \quad (C.2) \]

(Remembering that \( v_i(t) = v_i u(t) \) i.e. a step function of \( v_i \) volts.)

Equation C.2 becomes:

\[ I(s) = \frac{V_i}{R} \cdot \frac{1}{s + \frac{1}{RC}} \quad (C.3) \]

Taking inverse Laplace Transforms:
Appendix C. Relating to Signal Behaviour in Conductors

\[ i(t) = \frac{v_i}{R} e^{-\frac{t}{RC}} \]  

(C.4)

This gives an expression for the circuit's current response to a voltage step.

By inspection, Equation C.4 shows that the maximum current that will flow in the circuit is \( \frac{v_i}{R} \). This will occur as \( t \to 0 \) — when the voltage is first switched and the capacitor is effectively a short circuit. As time increases, this current will decay towards zero at an exponential rate determined by the value of the \( RC \) time constant.

\[
\begin{align*}
\text{Figure C-3: The derived Current Response to a Voltage Step for a simple RC Network.}
\end{align*}
\]

This is the derived current response (using Equation C.4), for a simple RC network. However, I wished to determine what the current response would be for a conducting wire.
C.3 Current in an RC Ladder Network

As mentioned previously, conductors are often modelled as RC ladder networks. This allows designers to assess signal propagation delays along the wire. Equations and approximations have been derived for this purpose [100].

The total resistance and capacitance can be calculated for a wire which is then split into \( n \) sections — these are the components of the ladder network (see Figure C-4). However such networks can be computationally difficult to analyse, especially as \( n \) increases. Ideally, \( n \to \infty \) for an accurate model.

HSPICE simulations were carried out to determine what trend the current spike would follow with a simple RC network, split into a ladder network, with an increasing number of sections (see Table C.3).

The voltage input was set as a single \( 0 \to +5V \) input with a rise time of approximately 1\( \text{ns} \).
It can be seen that as the number of sections increases, so does the maximum current flowing in the circuit. This current value may tend towards some limit as $n$ increases: What is this limit? If $n$ is very large then the simulation time will increase to an unacceptable level, and the files produced by HSPICE will swamp the disk space on the network!

More importantly, is increasing $n$ to some large number (say 1000), sufficient to model the conducting wire?
C.4 Current Modelling in a Conducting Wire

Equations have been derived to model electrical signal behaviour in conducting wires [101], [102], [103], [105].

These equations are known as the Transmission Line Equations, and model current and voltage in a conducting wire.

The conducting wire (Figure C-5), is modelled as having four electrical attributes:

![Diagram of electrical elements in a transmission line]

**Figure C-5**: Representation of the Electrical Elements in a Transmission Line.

- $R_l\Delta x$ - a resistance per unit length.
- $L_l\Delta x$ - an inductance per unit length.
- $C_l\Delta x$ - a capacitance per unit length.
- $G_l\Delta x$ - a leakage conductance per unit length.

The current and voltage through the wire are functions of time $t$ and the distance $x$ along the wire.
The transmission line equations for the wire (for voltage \(v(x,t)\) and current \(i(x,t)\) respectively), are:

\[
\frac{\partial^2 v}{\partial x^2} = \frac{1}{L_l C_l} \frac{\partial^2 v}{\partial t^2} + (R_l C_l + L_l G_l) \frac{\partial v}{\partial t} + R_l G_l v \tag{C.5}
\]

\[
\frac{\partial^2 i}{\partial x^2} = \frac{1}{L_l C_l} \frac{\partial^2 i}{\partial t^2} + (R_l C_l + L_l G_l) \frac{\partial i}{\partial t} + R_l G_l i \tag{C.6}
\]

Also,

\[
L_l \frac{\partial i}{\partial t} + R_l i = -\frac{\partial v}{\partial x} \tag{C.7}
\]

\[
C_l \frac{\partial v}{\partial t} + G_l v = -\frac{\partial i}{\partial x} \tag{C.8}
\]

In some circumstances these equations can be simplified. For example \(R_l\) and \(G_l\) may be negligible (as in the case of a lossless line).

In this case, \(L_l\) and \(G_l\) will be considered negligible (i.e. the \(R_l C_l\) effects dominate the line), so the equations become:

\[
\frac{\partial^2 v}{\partial x^2} = R_l C_l \frac{\partial v}{\partial t} \tag{C.9}
\]

\[
\frac{\partial^2 i}{\partial x^2} = R_l C_l \frac{\partial i}{\partial t} \tag{C.10}
\]

Current and voltage can also be written:

\[
\frac{\partial v}{\partial x} = -R_l i \tag{C.11}
\]

\[
\frac{\partial i}{\partial x} = -C_l \frac{\partial v}{\partial x} \tag{C.12}
\]
Appendix C. Relating to Signal Behaviour in Conductors

Equations C.9-C.12 are known as the Telegraph Equations.

Partial Differential Equations are difficult to solve. The equations require Boundary Conditions and initial conditions for a full solution.

The Boundary Conditions describe the known behaviour of the system at certain points. For example if the conducting wire (of length \( l \)), is grounded at both ends it can be said that:

\[
\begin{align*}
  v(0, t) & = 0 \\
  v(l, t) & = 0
\end{align*}
\]

That is — regardless of whatever value \( t \) takes — the voltage at each end of the cable will always be 0.

A system can have many different boundary and initial conditions (the wire may be open circuited at both ends, it may have an initial voltage distribution, etcetera), and a different solution exists for each set of these conditions. Defining the boundary conditions for a system can also be difficult!

C.4.1 Solving the Telegraph Equations for a Conducting Wire on a Silicon Chip to a Step Voltage Input

To solve the equations for such a system, it must be decided what conditions are at each end of the wire.

In this case, at the sending end of the wire, there is a voltage step function; at the receiving end of the wire there is an open-circuit.

There are several ways to solve Partial Differential Equations: taking Laplaceans, Separation of Variables, and other methods.

Several methods were initially attempted, using separation of variables and laplaceans. However, due to problems in defining the initial and boundary conditions, none of these methods proved satisfactory.
A solution was eventually found by making use of Heaviside’s *Operational Calculus* [104]. This methodology is similar to using Laplace Transforms.

**Solving the Equation**

Using Heaviside’s Operational Calculus, and letting \( x \) be measured from the receiving end of the line, Equations C.7 and C.8 can be written.

\[
\frac{\partial v}{\partial x} = (R_l + pL_i)i \tag{C.15}
\]

\[
\frac{\partial i}{\partial x} = (G_l + pC_i)v \tag{C.16}
\]

This gives:

\[
\frac{\partial^2 v}{\partial x^2} = (R_l + pL_i)(G_l + pC_i)v \tag{C.17}
\]

Letting: \( n^2 = -(R_l + pL_i)(G_l + pC_i) \).

Where \( n \) is a function of \( p \) and not of \( x \), C.15 can be written:

\[
\frac{\partial^2 v}{\partial x^2} + n^2 v = 0 \tag{C.18}
\]

This has the solution,

\[
v = A \cos nx + B \sin nx \tag{C.19}
\]

Writing: \( Z = R_l + pL_i \) gives,
\[ \frac{\partial v}{\partial x} = Zi \]  
\[ i = \frac{1}{Z} \frac{\partial v}{\partial x} \]  
\[ = \frac{n}{Z}(-A \sin nx + B \cos nx) \]

**Defining the Problem Conditions to Obtain a Solution** The Conditions are as follows:

- \( L_l \) and \( G_l \) are negligible.
- \( v = v_i u(t) \) at \( x = l \) (the sending end of the line).
- \( i = 0 \) at \( x = 0 \) since the line is open-circuited at this point (the end of the line).

If \( L_l \) and \( G_l \) are zero, then \( n^2 = -pR_lC_l \) and \( Z = R_l \).

From \( i = 0 \) at \( x = 0 \):

\[ 0 = \frac{n}{Z}(-A \sin 0 + B \cos 0) \]  
\[ 0 = \frac{n}{Z}B \]  
\[ \Rightarrow B = 0 \]

\( v = v_i \) at \( x = l \) gives:

\[ v = v_i = Acosnl \]  
\[ \Rightarrow A = \frac{v_i}{\cos nl} \]
Therefore,

\[ v = \frac{v_1 \cos nx}{\cos nl} \]  \hspace{2cm} (C.28)

Where \( n \) is some function of \( p \).

Heaviside's Expansion Theorem states:

\[ f(p) = \frac{f_1(p)}{f_2(p)} \leftrightarrow f(t) = \left( f_1(0) \frac{f_1(p)}{f_2(0)} + \sum_{p=a,b,c...} \frac{f_1(p)}{f_2(p)} \right) \]  \hspace{2cm} (C.29)

Where \( a, b, c... \) are the roots of \( f_2(p) \).

In this case...

\[ f_1(p) = \cos nx \]  \hspace{2cm} (C.30)

\[ f_2(p) = \cos nl \]  \hspace{2cm} (C.31)

\[ f_2(p) = 0 \]  \hspace{2cm} (C.32)

\[ \Rightarrow nl = \pm(2s + 1)\frac{\pi}{2}, \ s = 0, 1, 2... \]  \hspace{2cm} (C.33)

\[ n^2l^2 = (2s + 1)^2\frac{\pi^2}{4} \]  \hspace{2cm} (C.34)

\[ -pR_iC_l l^2 = (2s + 1)^2\frac{\pi^2}{4} \]  \hspace{2cm} (C.35)

\[ p = -\frac{(2s + 1)^2\pi^2}{4 R_i C_l l^2} \]  \hspace{2cm} (C.36)

Also, \( n = \frac{(2s + 1)\pi}{2l} \)  \hspace{2cm} (C.37)

An expression is now required for \( pf_2'(p) \).
\[ f'_2(p) = -l \frac{dn}{dp} \sin nl \]  
\[ n^2 = -pR_iC_i \]  
\[ 2n \frac{dn}{dp} = -R_iC_i \]  
\[ \Rightarrow f'_2(p) = \frac{R_iC_i l \sin nl}{2n}, \quad n = \frac{(2s + 1)\pi}{2} \]  
\[ p f'_2(p) = -\frac{nl \sin nl}{2} \]  
\[ = -\frac{(2s + 1)\pi}{4} \sin nl \]

The solution is:

\[ v(x, t) = v_i \left( \frac{f_1(0)}{f_2(0)} + \sum_{p=a,b,c,...} \frac{f_1(p)}{pf'_2(p)} e^{pt} \right) \]  
\[ = v_i \left( 1 + \sum_{s=0}^{\infty} \frac{\cos \frac{nx}{nl} \sin \frac{n\pi}{2}}{nl \sin \frac{n\pi}{2}} e^{pt} \right) \]  
\[ \text{and} \quad nl = \frac{2s + 1}{2} \pi \Rightarrow \sin nl = (-1)^s \]  
\[ = v_i \left( 1 - \frac{4}{\pi} \sum_{s=0}^{\infty} (-1)^s \frac{\cos \left( \frac{2s+1}{2l} \pi x \right) e^{-\frac{(2s+1)^2 \pi^2 t}{2R_iC_i^2}}}{2s + 1} \right) \]

This equation satisfies the defining partial differential Equation C.10, and the initial and boundary conditions for \( x = l \) and \( t = 0 \).

An expression for current can be obtained by applying Equation C.11.
\[ i = -\frac{1}{R_i} \frac{\partial v}{\partial x} \quad \text{(C.48)} \]

\[ = -\frac{2v_i}{R_t l} \sum_{s=0}^{\infty} (-1)^s \sin \left( \frac{2s + 1}{2l} \pi x \right) e^{-\frac{(2s+1)^2}{4R_tC_l t^2}} \quad \text{(C.49)} \]

When \( t = 0 \) and \( x = 1 \), then this becomes:

\[ i = -\frac{2v_i}{R_t l} \infty = \infty \quad \text{(C.50)} \]

This was tested against the RC network of \( n = 1000 \) in Section C.3 using HSPICE.

The rise time of the input was decreased (i.e. letting the input tend towards a step function), and the magnitude of the maximum current noted (see Table C.4.1).

<table>
<thead>
<tr>
<th>( t_r ) (ns)</th>
<th>( I_{max} ) (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>0.005</td>
</tr>
<tr>
<td>10</td>
<td>0.5</td>
</tr>
<tr>
<td>0.1</td>
<td>17.731</td>
</tr>
<tr>
<td>0.0001</td>
<td>1537.1</td>
</tr>
</tbody>
</table>

Table C-2: HSPICE Current Response of a 1000 Element RC Ladder Network with a decreasing input voltage rise-time.

It can be seen that as the rise time approaches zero, all the current is sunk through the first element in the RC network. Therefore:

\[ i \to \frac{v_i}{R_t/n} \quad \text{(C.51)} \]

And as \( n \to \infty \) and \( R_t/n \to 0 \), \( i \to \infty \).
Therefore it can be seen that a large RC ladder network simulated in HSPICE does not quite suffice to model current flow in a conducting wire — an infinite network would be required. The ladder network does not model the derived mathematical equation and it also limits the maximum current flowing in the system. In order to make the current infinite each resistive component would have to have zero resistance.

In practice though, voltage functions on conducting wires are not step functions: they have some finite rise time. What is required is to model the system for some realistic voltage function with a variable rise time.

### C.4.2 Solving the Telegraph Equation for a Conducting Wire on a Silicon Chip with a Rising Voltage Signal

The first approach to solving this problem was to decide what form the voltage signal would take. It was decided to model the input voltage as an exponential of the form:

\[
v_i(t) = v_i(1 - e^{-at})
\]

This allows the rise time to be modified by altering \(a\). The expression can also be easily represented in the Laplace domain.

**Using Heaviside's Operational Calculus**

A solution for an exponential voltage input can be derived by substituting Equation C.52 for \(v_i\) in Equation C.49.
\[ i = -v_i(1 - e^{-at}) \cdot \frac{2}{R_i l} \sum_{s=0}^{\infty} (-1)^s \sin \left( \frac{2s + 1}{2l} \pi x \right) e^{-\frac{(2s+1)^2}{4R_i C_i}l^2} \] (C.53)

\[ = -v_i(1 - e^{-at}) \cdot \frac{2}{R_i l} \sum_{s=0}^{\infty} (-1)^s e^{-\frac{(2s+1)^2}{4R_i C_i}l^2} \text{, } x = l \] (C.54)

Letting \( x = l \) (since we are interested in the sending end of the wire).

Equation C.54 is difficult(!) to examine analytically (i.e. to derive an expression for the maximum current), however it is possible to perform a numerical analysis.

Values for \( R_i = 20,000 \Omega m^{-1}, C_i = 8 F m^{-1}, l = 1000 \mu m, v_i = +5 V, \) and \( a = 16 \) were selected \(^2\) and a computer program was written to generate some data for \( i \). An upper limit of \( s = 1000 \) was chosen (above this limit the exponential value became negligible).

The data was plotted and can be seen in Figure C-6.

\(^2\) For ease of plotting, not as typical values.
This gives a numerically determined value for the maximum current: \( i = 0.1287853\, A \) (at \( t = 0.0217\, s \)).

This result was compared against an HSPICE simulation run on the 1000 element RC network with the same parameters. This yielded a maximum current of \( 0.24077\, A \) — a result almost twice as big.

As the number of elements in the network is increased the maximum current value also increases. This shows that increasing the size of the ladder network is the wrong approach for modelling current signals in wires.

Using Laplace Transforms

Because the expression derived using Heaviside’s Operational Calculus is difficult to analyse an attempt was made to derive an alternative — possibly simpler — expression by solving the system using Laplace Transforms. The following method is similar to a technique used in [106].

The voltage and current of the system can be written:
The initial conditions are defined as:

\[
I(x,0) = I_0(x) \quad (C.57)
\]
\[
V(x,0) = V_0(x), \quad t > 0 \quad (C.58)
\]

There is zero initial current and voltage on the line, and the current and voltage through the line is finite for all \(x\).

Taking Laplace Transforms of Equations C.55 and C.56 gives:

\[
(L_i s + R_i)I(x,s) = -\frac{dV(x,s)}{dx} + L_i I_0(x) \quad (C.59)
\]
\[
(C_i s + G_i)V(x,s) = -\frac{dI(x,s)}{dx} + C_i V_0(x) \quad (C.60)
\]

\(V(x,s), I(x,s)\) can be written:

\[
V(x,s) = \frac{1}{C_i s + G_i} \left\{ -\frac{dI(x,s)}{dx} + C_i V_0(x) \right\} \quad (C.61)
\]
\[
I(x,s) = \frac{1}{L_i s + R_i} \left\{ -\frac{dV(x,s)}{dx} + L_i I_0(x) \right\}^a \quad (C.62)
\]

\textsuperscript{a}Modified from [107] where it is misprinted.

And since \(\frac{dV(x,s)}{dx} = \frac{d}{dx} V(x,s)\), Equation C.59 becomes:
Appendix C. Relating to Signal Behaviour in Conductors

\[ \frac{d^2V}{dx^2} - q^2V = L\frac{dI_0}{dt} - C_i(L_is + R_i)V_0 \]  \hspace{1cm} (C.63)

Where:

\[ I = I(x, s), \ V = V(x, s), \ V_0 = V_0(x), \ I_0 = I_0(x), \ q^2 = (L_is + R_i)(C_is + G_i). \]

Since the initial condition of the wire is zero voltage and current, Equation C.63 becomes:

\[ \frac{d^2V}{dx^2} - q^2V = 0 \]  \hspace{1cm} (C.64)

The boundary conditions for the wire transform to:

\[ v(x, t) = v_i(1 - e^{-\alpha t}), \ x = 0 \rightarrow V(0, s) = \frac{v_i a}{s(s + a)} \]  \hspace{1cm} (C.65)

\[ i(x, t) = 0, \ x = 1 \rightarrow I(l, t) = 0 \]  \hspace{1cm} (C.66)

The general solution of Equation C.64 is:

\[ V = Ae^{-qx} + Be^{qx} \]  \hspace{1cm} (C.67)

Also, since \( I = -\frac{1}{Z} \frac{dV}{dx} \), \( Z = (L_is + R_i) \):

\[ I = -\frac{1}{Z}(-qAe^{-qx} + qBe^{qx}) \]  \hspace{1cm} (C.68)

We now wish to determine \( A \) and \( B \).

At \( x = 0 \),

\[ V = \frac{v_i a}{s(s + a)} \rightarrow A + B = \frac{v_i a}{s(s + a)} \]  \hspace{1cm} (C.69)
Appendix C. Relating to Signal Behaviour in Conductors

At $x = l$,

$$I = 0 \rightarrow -A + Be^{2ql} = 0 \quad \text{(C.70)}$$

So:

$$A = \frac{v_ia}{s(s + a)} \left( 1 - \frac{1}{1 + e^{2ql}} \right) \quad \text{(C.71)}$$

$$B = \frac{v_ia}{s(s + a)(1 + e^{2ql})} \quad \text{(C.72)}$$

And:

$$V = \frac{v_ia}{s(s + a)} \frac{1}{1 + e^{2ql}} \left( e^{2ql}e^{-qz} + e^{qx} \right) \quad \text{(C.73)}$$

$$I = \frac{1}{Z} \frac{v_ia}{s(s + a)} \frac{1}{1 + e^{2ql}} \left( -e^{2ql}e^{-qz} + e^{qx} \right) \quad \text{(C.74)}$$

For the VLSI case, it is assumed that $R_l$ and $C_l$ dominate and $L_l$ and $G_l$ are negligible, so:

$$q = \sqrt{sR_lC_l} , \ Z = R_l \quad \text{(C.75)}$$

Again letting $x = 0$ gives:

$$I = \sqrt{\frac{C_l}{R_l}}v_ia \frac{1}{\sqrt{s(s + a)}} \left( 1 - \frac{2}{e^{\sqrt{2}\sqrt{s}R_lC_l} + 1} \right) \quad \text{(C.76)}$$

Laplaceans of this sort are extremely difficult to transform into the time domain. Reference searches and internet queries proved fruitless as did the use of computer software (Xmaple).

\footnote{If not impossible!}
C.5 Conclusions

This chapter/appendix has shown that accurately analysing conducting lines is a non-trivial task. Using HSPICE simulations of ladder network approximations is not always sufficient depending on the accuracy required and may in fact be the wrong approach.

A (numerical) method of calculating the current flow in a conducting wire has been derived that will allow an estimation (bearing in mind that $L_i$ and $G_i$ have been neglected), of current behaviour to be made.

This estimation gives an $i_{\text{max}}$ value that is less than values determined by HSPICE simulations of RC ladder networks. Therefore sizing conductor widths based on such HSPICE simulations may guarantee a “safe” design (even if over-engineered).
Appendix D

Reference Materials downloaded from the WWW
Developed by TI and designed around our innovative Digital Micromirror Device (DMD), Digital Light Processing enables an all-digital approach to projection display from the initial data input, to processing and the final image display.

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2. **A typical DLP circuit board consists of analog-to-digital decoders, memory chips, a video processor and several digital signal processors (DSPs).** This is where the text, graphics and video are processed to yield a pure digital signal with tones and color values that rival the image quality of photographic film.

3. **sent to the heart of the DLP system – the DMD –**

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Price and performance combined in portable and small-audience projection systems.
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The input signal is broken down into RGB data. The data are sequentially written to the DMD's SRAM. A white light source is focused onto the color wheel through the use of condensing optics. The light that passes through the color wheel is then imaged onto the surface of the DMD. As the wheel spins, sequential red, green and blue light hits the DMD. The color wheel and video signal are in sequence so that when red light is incident on the DMD, the mirrors tilt on according to where and how much red information is intended for display. The same
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When a color wheel is used, two-thirds of the light is blocked at any given time. As white light hits the red filter, the red light is transmitted and the blue and green light is absorbed. The same holds true for the blue and green filters: the blue filter transmits blue and absorbs red and green, the green filter transmits green and absorbs red and blue.

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D.4 http://www.bnonlinear.com/LCref.htm

characteristics. A Smectic C* device typically modulates light similar to a passive half-wave retarder. The applied electric field results in a rotation of the half-wave retarder's slow-axis about the optic axis. Smectic C* devices have fast optical rise and fall times (~50-150 microseconds). Smectic C* devices do respond to the polarity of the applied electric field. This results in an "inverse" image when the inverse frame is written in order to maintain the DC balance. For some applications, such as optical correlation utilizing binary phase-only modulation, this inverse image is identical to the "true" image and can therefore still be utilized. For other applications, the illumination source or detector should be pulsed to avoid "seeing" the inverse image.

- Typical configuration - Smectic C* cell with layer thickness equivalent to a half-wave of retardance at the desired wavelength.
- Modulation - applied electric field will result in a rotation of the slow-axis of the half-wave retarder, this will rotate a linearly polarized input beam or add/subtract phase to a circularly polarized input beam
- Range - typically 0° with maximum negative voltage to 45° with maximum positive voltage, range can be as large as 90° with newer Smectic C* mixtures
- Speed - 50-150 microseconds, 10% - 90% of modulation depth, temperature and wavelength dependent, most visible wavelength, reflection mode devices will respond in ~75 microseconds

Smectic A*

Smectic A* devices are used only when very high switching speeds are required. These devices must be operated at elevated temperatures and typically exhibit short lifetimes relative to Nematic or Smectic C* devices. A Smectic A* device can have optical rise and fall times as fast as 200 ns. These devices can exhibit tilt angles as high as ±50° but not at elevated speeds. Smectic A* devices modulate light in a similar fashion to the Smectic C* devices, i.e. a rotating retarder.

- Typical configuration - Smectic A* cell with layer thickness equivalent to a half-wave of retardance at the desired wavelength.
- Modulation - applied electric field will result in a rotation of the slow-axis of the half-wave retarder about the surface normal of the device, this will rotate a linearly polarized input beam or add/subtract phase to a circularly polarized input beam
- Range - typically 0° with maximum negative voltage up to 50° with maximum positive voltage
- Speed - 200-900 ns, 10% - 90% of modulation depth, temperature and wavelength dependent, must be operated at elevated temperatures

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fax : +44 (0)181 848 6565
e-mail : lbanks@crl.co.uk
What are Liquid Crystals?

Liquid crystals are a phase of matter whose order is intermediate between that of a liquid and that of a crystal. The molecules are typically rod-shaped organic moieties about 25 Angstroms in length and their ordering is a function of temperature. The nematic phase, for example, is characterized by the orientational order of the constituent molecules. The molecular orientation (and hence the material's optical properties) can be controlled with applied electric fields. Nematics are (still) the most commonly used phase in liquid crystal displays (LCDs), with many such devices using the twisted nematic geometry.

The smectic phases, which are found at lower temperatures than the nematic, form well-defined layers that can slide over one another like soap. The smectics are thus positionally ordered along one direction. In the Smectic A phase, the molecules are oriented along the layer normal, while in the Smectic C phase they are tilted away from the layer normal. These phases, which are liquid-like within the layers, are illustrated below. There are also tilted phases which have hexatic in-plane ordering, like the Smectic I and Smectic F, as well as various crystalline smectics.

Of particular interest are tilted phases of chiral molecules, which possess permanent polarizations and are thus ferroelectric. These ferroelectric liquid crystals (FLCs) respond much more quickly to applied fields than nematics do and can be used to make fast, bistable electro-optic devices called Surface-Stabilized Ferroelectric Liquid Crystals (SSFLCs).

Are you east of the Atlantic Ocean? It may be faster for you to access this tutorial material from a mirror site maintained by the Heppke Group at the Technical University in Berlin. Both English and
Appendix D. Reference Materials downloaded from the WWW

D.7  http://liqcryst.chemie.uni-hamburg.de/

Liquid Crystal Group Hamburg

LiqCryst - the Database of Thermotropic Liquid Crystals

Liquid crystals cover a wide range of chemical structures, including rod-like molecules, disc-like molecules, amphiphilic materials, cellulose derivatives, metallomesogens, steroids, glycolipids, NLO compounds, etc.

Typical applications for liquid crystals are LCD displays, surfactants, membranes, color pigments, advanced materials, photoconductors etc.

The database LiqCryst compiles chemical structures, thermal phase behavior, physical properties and references of all known thermotropic liquid crystals.

The program has QSAR methods and prediction functions for physical properties.

- LiqCryst 2.1 - Database of Liquid Crystalline Compounds
- LiqCryst for Polymers
- LiqCryst 3.0 - Database of Liquid Crystalline Compounds
- Frequently Asked Questions about LiqCryst
- LiqCryst im WebDoc
- Request further Information / Request for Demo Version

Data on Liquid Crystalline Compounds


**Liquid Crystal Primer**

(Orders immediately to pictorial tutorial)

Ordinary fluids are isotropic in nature: they appear optically, magnetically, electrically, etc. to be the same from any perspective. Although the molecules which comprise the fluid are generally anisometric in shape, this anisometry generally plays little role in anisotropic macroscopic behavior (aside from viscosity). Nevertheless, there exists a large class of highly anisometric molecules which gives rise to unusual, fascinating, and potentially technologically relevant behavior. There are many interesting candidates for study, including polymers, micelles, microemulsions, and materials of biological significance, such as DNA and membranes. Although at times we have investigated all of these materials, our primary effort centers on liquid crystals.

Liquid crystals are composed of moderate size organic molecules which tend to be elongated and shaped like a cigar, although we have studied, and the literature is full of variety of other, highly exotic shapes as well. Because of their elongated shape, under appropriate conditions the molecules can exhibit orientational order, such that all the axes line up in a particular direction. In consequence, the bulk order has profound influences on the way light and electricity behave in the material. For example, if the direction of the orientation varies in space, the orientation of the light (i.e., the polarization) can follow this variation. A well-known application of this phenomenon is the ubiquitous liquid crystal display, now comprising a $15b$ annual industry world-wide. Under other conditions the molecules may form a stack of layers along one direction, but remain liquid like (in terms of the absence of translational order) within the layers. As the system changes from one of these phases to another, a variety of physical parameters such as susceptibility and heat capacity, will exhibit "pretransitional behavior. Based solely on symmetry, this behavior may be related to other physical systems, such as superconductivity, magnetism, or superfluidity; this is the so-called "universality" of these phase transitions.

Using a battery of optical techniques, in addition to dielectric and certain surface probes, our research centers on the role of symmetry on liquid crystalline phases and phase transitions, how these systems behave in the presence of intense magnetic and electric fields, and the effects of confining these materials in spaces not much larger than the molecules themselves. By observing this behavior, we learn not only about the particular material under consideration, but about the global properties of anisotropic fluids and their relationships to other physical systems. Finally, we should point out that although our research is primarily fundamental in nature, determining critical exponents, surface potentials, induced polarizations, etc., a small but important component of our effort involves technology. For example, we have developed a new liquid crystal display architecture which is being developed for commercialization by American industry. This is a symbiotic approach to research, and has been an intellectual stimulation to our effort.

**Typical Liquid Crystalline Molecules:**

\[
\begin{align*}
\text{Methoxybenzilidene Butylaniline (MBBA)} \\
\text{CH}_3 \\
\text{O} \\
\end{align*}
\]

p-decyloxybenzilidene p'-amino 2-methylbutylcinnamate ("DOBAMBC")

**A Physicist's View:**

For many applications, a liquid crystal molecule is often pictured as a rod. This view will often provide important qualitative information about the macroscopic behavior of the system, but will overlook many nuances and sometimes important macroscopic features. For example, the chiral nature of DOBAMBC [above] permits the molecule to exhibit a "ferroelectric phase" [see below]. The size of the polarization and the response of the molecule to an applied voltage depends on the chemical structure of the molecule, largely the carbonyl [C=O] group near the chiral carbon.

**Isotropic Phase**

- In the isotropic phase the molecules are randomly aligned and exhibit no long range order.

The isotropic phase has a low viscosity and will often appear to be crystal clear. There is no long range positional or orientational order of the molecules, although this sort of order may exist on very short length scales of order tens of Angstroms, corresponding to a few molecular distances. For all practical purposes, the isotropic phase macroscopically appears to be like any other isotropic liquid such as water.
Nematic Phase

The molecules in the nematic phase are oriented on average along a particular direction. In consequence, there is a macroscopic anisotropy in many material properties, such as dielectric constants and refractive indices. This is the phase which is used in many liquid crystal devices (e.g., the "twisted nematic" cell), because the average orientation may be manipulated with an electric field, and the polarization of light will follow the molecular orientation as it changes through a cell. Typical response times are in the millisecond range.

Smectic A Phase

The smectic phase A, like the nematic, exhibits long range orientational order of the molecules. In addition, it exhibits a layer like structure in one dimension, and thus is often considered a two dimensional liquid (freedom of molecular motion within the layer) and a quasi one-dimensional solid (hindered translation from one layer to the next). The viscosity is rather high, and this phase is generally not useful for devices.

(Tilted) Smectic C Phase

In this phase the molecules are tilted with respect to the layers, and the system is now "biaxial" in character.

Smectic C* (Chiral) - Ferroelectric

If the molecules are chiral, (lack inversion symmetry), Meyer, et al demonstrated on symmetry grounds that a polarization must exist parallel to the smectic layers and perpendicular to the molecules. The magnitude of the polarization is determined by molecular considerations, although its existence depends solely on symmetry. These materials can be used in rapidly switching electrooptic shutters, with response times in the microsecond range.

Antiferroelectric LCs
Antiferroelectric liquid crystals are similar to ferroelectric liquid crystals, although the molecules tilt in an opposite sense in alternating layers. In consequence, the layer-by-layer polarization points in opposite directions. These materials are just beginning to find their way into devices, as they are fast, and devices can be made "bistable."
Introduction to Liquid Crystals

The study of liquid crystals began in 1888 when an Austrian botanist named Friedrich Reinitzer observed that a material known as cholesteryl benzoate had two distinct melting points. In his experiments, Reinitzer increased the temperature of a solid sample and watched the crystal change into a hazy liquid. As he increased the temperature further, the material changed again into a clear, transparent liquid. Because of this early work, Reinitzer is often credited with discovering a new phase of matter - the liquid crystal phase.

Liquid crystal materials are unique in their properties and uses. As research into this field continues and as new applications are discovered, liquid crystals are sure to become an important part of modern technology. This tutorial provides an introduction to the science and applications of these special materials.

What are Liquid Crystals?

Materials that show liquid crystal behavior generally have several common characteristics. Among these are a rod-like molecular structure, a rigidity of the long axis, and strong dipoles and/or easily polarizable substituents.

The distinguishing characteristic of the liquid crystalline state is the tendency of the molecules to point along a common axis called the director. This degree of order is responsible for the unique behavior of the material. In contrast, molecules in the liquid phase have no intrinsic order. In the solid state, molecules are highly ordered and have little translational freedom. The characteristic orientational order of the liquid crystal state is found between the traditional solid and liquid phases. Note the average alignment of the molecules for each phase in the following diagram.

It is sometimes difficult to determine whether a material is in a crystal or liquid crystal state. Crystalline materials demonstrate long range periodic order in three dimensions. Substances that do not have this degree of positional order but do show more than an isotropic liquid are properly called liquid crystals.

To gauge the average alignment of a material, an order parameter (S) is defined. The equation for the traditional order parameter is as follows:

$$ S = \langle \cos \theta \rangle = \frac{1}{2} < 3 \cos^2 \theta - 1 > $$

where $\theta$ refers to the angle between the director and the long axis of each molecule. The brackets around the cosine term denote an average over all of the molecules. In an isotropic liquid, the average of the cosine terms will disappear producing an order parameter equal to zero. For a perfectly aligned liquid crystal, the order parameter evaluates to one. The order parameter of a material varies inversely with temperature as a result of kinetic molecular motion. Typical values for the order parameter of a liquid crystal range between 0.3 and 0.9.

The tendency of the liquid crystal molecules to point along the director leads to a condition known as anisotropy. This term means that the properties of a material depend on the direction in which they are measured. For example, the index of refraction of light may vary with respect to the viewing angle in an anisotropic material. It is the anisotropic nature of liquid crystals which enables scientists and engineers to use these materials in a variety of commercial applications.

Characterizing Liquid Crystals

The following parameters describe the liquid crystalline structure:

1. Positional Order
2. Bond Orientational Order
3. Molecular Orientation

The extent to which an average molecule or group of molecules shows translational symmetry (i.e. they move together) is called positional order. Bond orientational order describes not only how the molecules are packed in a two-dimensional system, but the orientation of a bond joining nearest-neighbor centers of mass. Molecular orientation is a measure of the tendency of the molecules to align along the director.

Most liquid crystal compounds exhibit polymorphism or a condition where more than one phase is
observed in the liquid crystalline state. The term mesophase is used to describe the "subphases" of liquid crystal materials. Mesophases are formed by either imposing order in only one or two specific dimensions or by allowing the molecules to have a degree of translational motion. The following sections will go into greater detail of the mesophases of liquid crystals.
What are Ferroelectric Liquid Crystals?

The Nematic and Smectic A (SA) liquid crystal phases are too symmetric to allow any vector order, such as ferroelectricity. The tilted smectics, however, do allow ferroelectricity if they are composed of chiral molecules. The pictures below (they’re clickable) show the original ferroelectric LC, DOBAMBC and a modern compound, W 314:

In the simplest case, the Smectic C (SC), the average long molecular axis is tilted from the layer normal z by a fixed angle but the molecules are free to rotate on the so-defined tilt cone. The phase has a C2 symmetry axis perpendicular to both the molecular director and the layer normal. The molecules exhibit a net spontaneous polarization along this axis. The magnitude of the polarization depends on temperature, generally decreasing as the tilt angle goes to zero at the SC - SA phase transition. The following Figure shows the geometry of the chiral SC phase:

Ferroelectric liquid crystals (FLCs) also exhibit a spontaneous helixing of the polarization, so that over macroscopic distances (a few microns, say) the polarization averages to zero.

Since the coupling of the polarization to applied fields is linear in the field, this means that FLCs can be made to switch quickly (typically within a few microseconds) and in a bipolar manner. This makes FLCs ideally suited to electrooptic applications. FLCs are now included in several display technologies, the most popular of which use the surface-stabilized (SSFLC) geometry.
Liquid Crystal Phases

The liquid crystal state is a distinct phase of matter observed between the crystalline (solid) and isotropic (liquid) states. There are many types of liquid crystal states, depending upon the amount of order in the material. This section will explain the phase behavior of liquid crystal materials.

Nematic Phases

The nematic liquid crystal phase is characterized by molecules that have no positional order but tend to point in the same direction (along the director). In the following diagram, notice that the molecules point vertically but are arranged with no particular order.

![A theoretical representation of the nematic phase (left) and a photo of a nematic liquid crystal](image)

[Image: A theoretical representation of the nematic phase (left) and a photo of a nematic liquid crystal]

Liquid crystals are anisotropic materials, and the physical properties of the system vary with the average alignment with the director. If the alignment is large, the material is very anisotropic. Similarly, if the alignment is small, the material is almost isotropic.

The phase transition of a nematic liquid crystal is demonstrated in the following movie. The nematic phase is seen as the marbled texture. Watch as the temperature of the material is raised, causing a transition to the black, isotropic liquid.

![Movie](https://example.com/movie)

A special class of nematic liquid crystals is called chiral nematic. Chiral refers to the unique ability to selectively reflect one component of circularly polarized light. The term chiral nematic is used interchangeably with cholesteric. Refer to the section on cholesteric liquid crystals for more information about this mesophase.

Smectic Phases

The word "smectic" is derived from the Greek word for soap. This seemingly ambiguous origin is explained by the fact that the thick, slippery substance often found at the bottom of a soap dish is actually a type of smectic liquid crystal.

The smectic state is another distinct mesophase of liquid crystal substances. Molecules in this phase show a degree of translational order not present in the nematic. In the smectic state, the molecules maintain the rotational symmetry of nematics, but also tend to align themselves in layers or planes. Motion is restricted to within these planes, and separate planes are observed to flow past each other. The increased order means that the smectic state is more "solid-like" than the nematic.

Many compounds are observed to form more than one type of smectic phase. As many as 12 of these variations have been identified, however only the most distinct phases are discussed here.

In the smectic-A mesophase, the director is perpendicular to the smectic plane, and there is no particular positional order in the layer. Similarly, the smectic-B mesophase orients with the director perpendicular to the smectic plane, but the molecules are arranged into a network of hexagons within the layer. In the smectic-C mesophase, molecules are arranged as in the smectic-A mesophase, but the director is at a constant tilt angle measured normally to the smectic plane.

As in the nematic, the smectic-C mesophase has a chiral state designated C*. Consistent with the smectic-C, the director makes a tilt angle with respect to the smectic layer. The difference is that this angle rotates from layer to layer forming a helix. In other words, the director of the smectic-C mesophase is not parallel or perpendicular to the layers, as in the smectic-C* mesophase, it rotates from one layer to the next. Notice the twist of the director, represented by the green arrows, in each layer in the following diagram.
External Influences on Liquid Crystals

Scientists and engineers are able to use liquid crystals in a variety of applications because external perturbation can cause significant changes in the macroscopic properties of the liquid crystal system. Both electric and magnetic fields can be used to induce these changes. The magnitude of the fields, as well as the speed at which the molecules align are important characteristics industry deals with. Finally, special surface treatments can be used in liquid crystal devices to force specific orientations of the director.

Electric and Magnetic Field Effects

The response of liquid crystal molecules to an electric field is the major characteristic utilized in industrial applications. The ability of the director to align along an external field is caused by the electric nature of the molecules. Permanent electric dipoles result when one end of a molecule has a net positive charge while the other end has a net negative charge. When an external electric field is applied to the liquid crystal, the dipole molecules tend to orient themselves along the direction of the field. In the following diagram, the black arrows represent the electric field vector and the red arrows show the electric force on the molecule.

![Electric field diagram]

Even if a molecule does not form a permanent dipole, it can still be influenced by an electric field. In some cases, the field produces slight re-arrangement of electrons and protons in molecules such that an induced electric dipole results. While not as strong as permanent dipoles, orientation with the external field still occurs.

The effects of magnetic fields on liquid crystal molecules are analogous to electric fields. Because magnetic fields are generated by moving electric charges, permanent magnetic dipoles are produced by electrons moving about atoms. When a magnetic field is applied, the molecules will align with the field.

Surface Preparations

In the absence of an external field, the director of a liquid crystal is free to point in any direction. It is possible, however, to force the director to point in a specific direction by introducing an outside agent to the system. For example, the glass plates usually employed to observe liquid crystals may be specially treated so that the molecules near the surface align themselves in a certain direction. The reasons for this "anchoring" due to the surface preparation are not well understood and are currently being researched.

The competition between orientation produced by surface anchoring and by electric field effects is often exploited in liquid crystal devices. Consider the case in which liquid crystal molecules are aligned parallel to the surface and an electric field is applied perpendicular to the cell as in the following
What are Surface-Stabilized Ferroelectric Liquid Crystals?

Although the molecular director in bulk ferroelectric liquid crystals (FLCs) adopts a helical structure, Noel Clark and Sven Lagerwall [photograph] found in 1980 that by confining the LC material between closely-spaced glass plates (spaced closer than the ferroelectric helix pitch), the natural helix could be suppressed. This principle is illustrated in the polarized micrograph above, where helix lines are largely absent in the thinner (upper right) part of the cell. Clark and Lagerwall found that the smectic layers were oriented approximately perpendicular to the glass. Furthermore, they discovered that such cells could be switched rapidly between two optically distinct, stable states simply by alternating the sign of an applied electric field.

It has since been established by Clark's group that there are two commonly found layer geometries, called bookshelf and chevron, the latter being portrayed in the Figure above. The electro-optic properties of an SSFLC depend strongly on the layer geometry as well as on the nature of the orienting properties of the bounding glass plates. Some images of SSFLC textures may be seen on another page.

SSFLCs are being studied in many research laboratories throughout the world. They form the basis for the development of optical shutters, phase plates, and high-resolution color displays.
crystalline (C), liquid crystalline (N = nematic, see below), and isotropic (I) state given in Fig. 2 are in Celsius.

**liquid crystalline phases**

![Nematic and Cholesteric Structures](image)

Fig. 3: liquid crystalline mesophases

Some mesophases of calamitic molecules are schematically drawn in Fig. 3. In the simplest case the molecules possess only orientational but no positional long range order. Liquid crystals of that type are called nematic (from Greek nemos = thread), the name of which has been given with respect to thread-like textures observed under polarizing microscope. The direction of preferred alignment can be described by a unit vector, the so-called nematic director \( \hat{\mathbf{e}} \). In practice, the orientation of individual molecules differs significantly from that direction, and the director must be more correctly defined as the symmetry axis of the orientational distribution. In nematics the distribution function is rotationally symmetric around the director, i.e. they are uniaxial.

If a nematic liquid crystal is made of chiral molecules, i.e. the molecules differ from their mirror image, a cholesteric liquid crystal (from cholesterol acetate, the first kind of this type) is obtained. Locally, cholesterics can be practically not distinguished from nematics but the preferred orientation forms a helical structure, with the helical axis perpendicular to the director.

The smectic phases (from Greek smegma = soap) are characterized by additional degrees of positional order. Generally, the molecules are arranged in layers in these mesophases, which can be considered as one-dimensional density waves. In smectic A (SmA) liquid crystals the molecular orientation is perpendicular to the layers, whereas the director is tilted in the SmC phase. Both show no positional order within the layers and therefore are often considered as two-dimensional liquids. The SmC phase of chiral molecules may form a helical structure which is denoted as SmC*. There are further smectic phases with weak cubic or hexagonal positional order within the layers, which will not be discussed here.

**unique properties**

![Diagram of Anisotropic Fluids](image)

Fig. 4: physical properties of liquid crystals

As a result of orientational order, most physical properties of liquid crystals are anisotropic and must be described by second rank tensors. Examples are the heat diffusion, the magnetic susceptibility, the dielectric permittivity or optical birefringence. Additionally, there are new physical quantities, which do not appear in simple liquids as e.g. elastic or frictional torques (rotational viscosity) acting on static or dynamic director deformations, respectively.

The most remarkable features of liquid crystals with respect to applications are due to their anisotropic optical properties. Nematics, and SmAs are uniaxial, SmCs weakly biaxial. Cholesterics give rise to
The following figure shows a typical binary hologram and its Fourier transform.

![Hologram Image]

Since Dames et al. introduced this technique it became the basic technique for calculation of binary and multi-phase level fan-out holographic elements. The solutions obtained using this method do not usually resemble the distribution of complex output obtained by taking the Fourier transform of the intensity distribution in the object plane. There can exist several different patterns which produce outputs of similar quality and efficiency.

**Four phase holograms**

The four phase hologram design technique is similar to the one for binary structures. The main advantage of using multi-phase holograms is the absence of a conjugate image in the output field area. A four-phase hologram can be described by a formula:

\[
F(k,l) = \sum_{m,n} f(m,n)e^{4\pi/(2k)}
\]

The possible four values of a pixel transmittance \(f(m,n)\) are: \(\pm 1\) and 0. Since the pixels of the hologram can be flipped into any of 4-phase states compared to 2 for binary holograms the computational time is two times longer.

A possible fabrication method for four-phase holograms is described in involves electron beam lithography and subsequent dry etching of the pattern into four phase levels on silica glass substrates. It is also possible to implement these holograms dynamically on two SLMs, but such an optical system would be very expensive and difficult to align due to diffraction effects. The surfaces of the SLMs should be as close as possible to each other to achieve acceptable results which is technologically a difficult task. In order to successfully implement a fully dynamic four-phase level hologram and benefit from its high performance and the absence of a secondary image it is possibly needed to create a new type of 2-layered SLM device.

**Connected holograms**

The use of binary holograms may be considerably enhanced if they can be electrically switched. It is possible to make such a device by arranging that the phase modulation is introduced through changing the optical properties of a layer of liquid crystal by applying a spatially modulated electric field. This requires that the phase modulation pattern desired is electrically connected over the spatial extent of the structure. Electrically switchable liquid crystal lenses using patterned electrodes have been reported. The device comprises a liquid crystal cell sandwiched between two glass optical flats. The glass backplane is uniformly coated with a transparent electrode such as indium tin oxide (ITO). The front plate is patterned, again with ITO, with the required connected structure. On application of a potential between front and back plates the liquid crystal undergoes a spatially variant phase modulation corresponding to the patterned front electrode.

In the switchable lens devices various methods have been used to ensure electrical connectivity in the phase pattern required, from a simple bar connecting the rings in a Fresnel zone plate, to using the intrinsic connected structure of a binary Gabor zone plate. Such switchable lenses have applications in imaging, scanner systems, detector protection elements and as optical interconnects.

I will introduce a new approach to the design of CGHs where the electrical connectivity requirement is incorporated as a constraint in the iterative algorithm. Liquid crystal devices fabricated using these holographic electrode patterns have the potential for producing high speed switching and the cell structure allows simple electronic addressing to enable the device. Such predefined fan-out, switchable holograms may have applications in systems where a fixed, predefined, set of optical interconnections are required, such as in optical databases, neural networks, and telecommunications. The speed and easier fabrication may make them more attractive than fully reconfigurable CGHs, written on spatial light modulators, for some applications.

**Requirements and implementation of continuity algorithm**

The design approach is based on the two-dimensional iterative scheme proposed by Dames et al.. As in Dames's scheme the connected structure minimisation is formed by choosing a pixel at random. Then the algorithm tests to see if the pixel should be switched on (set to +1) or off (set to -1) by using the following rules:

1. Switching off the pixel must not break the continuity of the existing pattern. If there are pixels in
O Scanning can be realised effectively only within a restricted angle.

The scanning speed is relatively low. This can be very low when gratings are calculated dynamically for each position of the beam (0.1-1 sec). If predefined gratings are used the scanning frequency is determined by the switching time of the SLM (up to 1 kHz).

Low efficiency (less than 45%) for binary holograms due to the secondary conjugate image. Generally speaking, pseudo-four phase sandwich holograms do not improve the efficiency because they simply spread the secondary image over the output area without contributing into the main image.

The laser beam steering can be described as one of the applications of optical interconnects. In the next section I will introduce an scheme for optical interconnects using SLMs and discuss some problems of its implementation which are also relevant to beam scanning.

**Optical interconnects.**

Optical information channels have extremely high bandwidths, can transfer information across free space, and do not suffer cross talk when they encounter another beam of light. One simple example of optical interconnects is the optical crossbar developed by Goodman. The scheme is shown in fig.3.7. This is a vector-matrix multiplier crossbar. The device transfers each input channel into a column of an interconnect shutter and the transmitted light from a row is focused onto an output channel.

Another device is shown on fig.3.8. This is a matrix-matrix crossbar switch that works in two dimensions [31, 32]. It improves the scalability of the previous device by avoiding the use of cylindrical lenses. The two NxN matrices are interconnected via an N2xN2 shutter matrix which is implemented on SLM. The input matrix is replicated using a holographic beam splitter. Each copy is multiplied by an SLM matrix and then focused onto an output matrix.
from ODE ON INTIMATIONS OF IMMORTALITY FROM RECOLLECTIONS OF EARLY CHILDHOOD
by William Wordsworth

Our birth is but a sleep and a forgetting;
The Soul that rises with us, our life’s Star,
    Hath had elsewhere its setting
    And cometh from afar;
    Not in entire forgetfulness
    And not in utter nakedness,
But trailing clouds of glory do we come
    From God who is our home:
Heaven lies about us in our infancy!
Shades of the prison-house begin to close
    Upon the growing Boy
But he beholds the light, and whence it flows,
    He sees it in his joy;
The Youth who daily farther from the east
    Must travel, still is Nature’s priest,
And by the vision splendid
    Is on his way attended;
At length the Man perceives it die away,
And fade into the light of common day.